ELECTRONICS - SEMICONDUCTOR

INTRODUCTION

The word "electronics' is derived from electron+dynamics which means the study of the behaviour of an electron under different conditions of externally applied fields.

This field of science deals with electronic devices and their utilization. An electronic device is a device in which conduction takes place by the movement of electron - through a vacuum, a gas or a semiconductor.

Some familiar devices are :

(i) Rectifier (ii) Amplifier (iii) Oscillator etc.

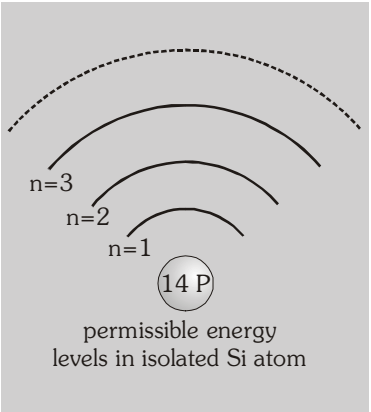
- **Application of Electronics**

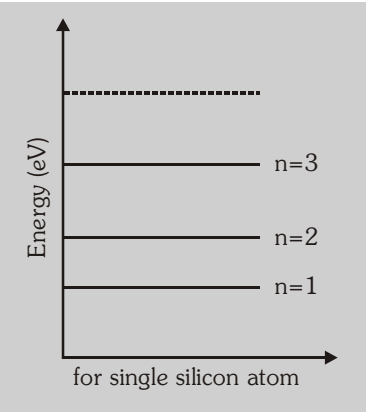
Communication	Entertainment	Defence	Medical
Telephone	TV Broadcast	Radar	X-rays
Telegraph	Radio Broadcast	Guided missiles	Electro cardio graph (ECG)
Mobile phone	VCR, VCD		CRO display
FAX			E.E.G. (Electro Engio Graph)
FM mic			

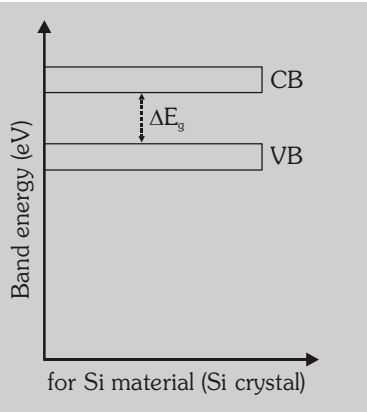
- Main application of electronics is computer which is used in every field.
- All electronics equipments required D.C. supply for operation (not A.C. supply)

- **ENERGY BAND THEORY**

Based on Pauli's exclusion principle







In an isolated atom, electrons are present in sharply defined energy levels. But in solids atoms are very close to each other. So because of their interactions, each electron doesn't have fixed energy.

It has different energy levels in a certain (small) range called energy band.

The number of energy levels in a band depends upon the number of interacting atoms.

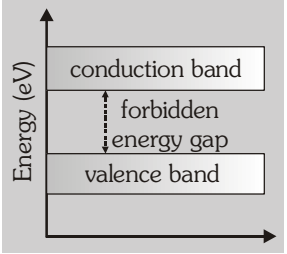
The energy band including valence electrons is called valence band (VB) and the energy band including conducting (free) electrons is called conduction band (CB).

- **Band gap or Forbidden Energy gap (FEG) (ΔE_g)**

$$\Delta E_g = (C B)_{min} - (V B)_{max}$$

(i) It is the energy gap between CB and VB.

(ii) It is also called forbidden energy gap because free electrons can not exist in this gap.



(iii) Width of forbidden energy gap depends upon the nature of substance.

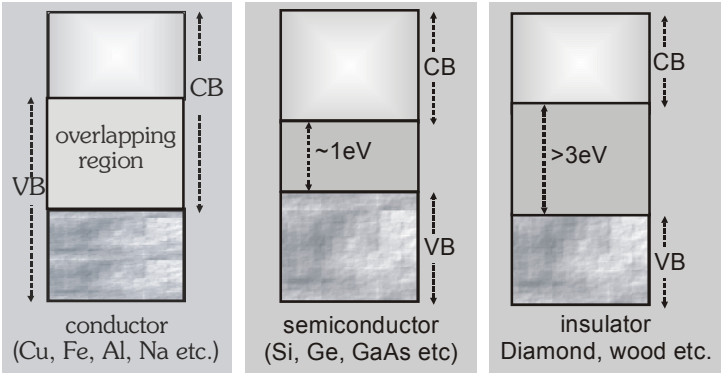
(iv) Width is more, then valence electrons are strongly attached with nucleus.

(v) Width of forbidden energy gap is represented in eV.

(vi) As temperature increases forbidden energy gap decreases (very slightly).

CLASSIFICATION OF SOLIDS ACCORDING TO ENERGY BAND THEORY

According to energy band theory, solids are conductor, semiconductor and insulator :



- **Conductor**

In some solids conduction band and valence band are overlapped so there is no band gap between them, it means $\Delta E_g = 0$.

Due to this a large number of electrons are available for electrical conduction and therefore its resistivity is low ($\rho = 10^{-2} - 10^{-8}\ \Omega$–m) and conductivity is high [$\sigma = 10^{2} - 10^{8}\ (\Omega\text{–m})^{-1}$]

Such materials are called conductors. For example gold, silver, copper etc.

- **Insulator**

In some solids energy gap is large ($E_g > 3$ eV).

So in conduction band there are no electrons and so no electrical conduction is possible. Here energy gap is so large that electrons cannot be easily excited from the valence band to conduction band by any external energy (electrical, thermal or optical).

Such materials are called as "insulator". Their $\rho > 10^{11}\ \Omega$–m and $\sigma < 10^{-11}\ (\Omega\text{–m})^{-1}$

- **Semiconductor**

In some solids a finite but small band gap exists ($E_g < 3$eV).

Due to this small band gap some electrons can be thermally excited to "conduction band".

These thermally excited electrons can move in conduction band and can conduct current. Their resistivity and conductivity both are in medium range, $\rho \simeq 10^{-5} - 10^{6}\ \Omega$–m and $\sigma \simeq 10^{-6} - 10^{5}\ \Omega\text{–m}^{-1}$

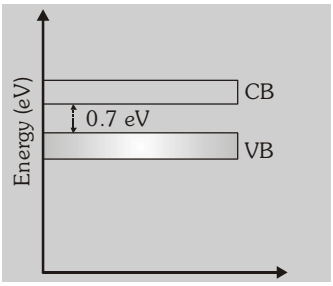
- **Example of semiconducting materials**

Elemental semiconductor :	Si and Ge	
Compound semiconductor	• Inorganic :	CdS, GaAs, CdSe, InP etc.
	• Organic :	Anthracene, Doped pthalocyanines etc.
	• Organic polymers :	Poly pyrrole, Poly aniline, polythiophene

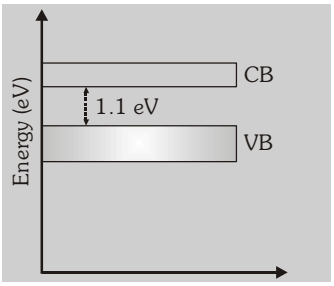
PROPERTIES OF SEMICONDUCTOR

- Negative temperature coefficient (α), with increase in temperature resistance decreases.
- Crystalline structure with covalent bonding [Face centred cubic (FCC)].
- Conduction properties may change by adding small impurities.
- Position in periodic table → IV group (Generally)
- Forbidden energy gap (0.1 eV to 3 eV)
- Charge carriers : electron and hole.
- There are many semiconductors but few of them have practical application in electronics like

Ge^{32} : 2, 8, 18, 4



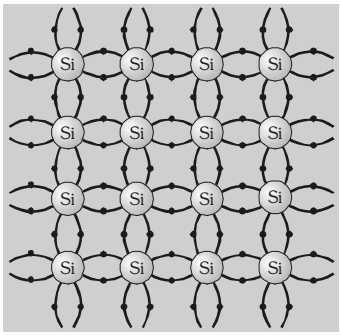
Si^{14} : 2, 8, 4



Effect of temperature

At absolute zero kelvin temperature

At this temperature covalent bonds are very strong and there are no free electrons and semiconductor behaves as perfect insulator.

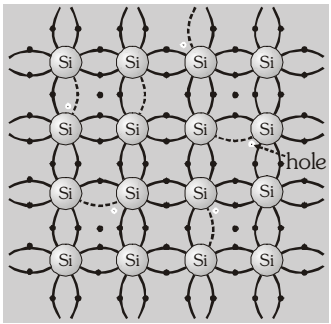


at 0 K

valence band fully filled | conduction band fully empty

Above absolute temperature

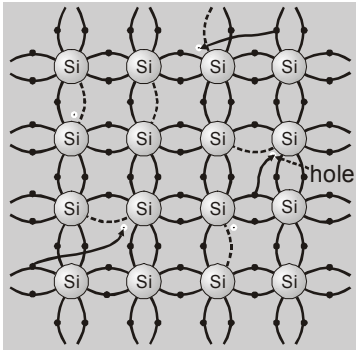
With increase in temperature some covalent bonds are broken and few valence electrons jump to conduction band and hence it behaves as poor conductor.



at higher temperature

valence band partially empty | conduction band partially filled

CONCEPT OF "HOLES" IN SEMICONDUCTORS



Due to external energy (temperature or radiation) when electron goes from valence band to conduction band (i.e. bonded electrons becomes free), vacancy of free e^- creates in valence band. The electron vacancy called as"hole" which has same charge as electron but positive. This positively charged vacancy move randomly in semiconductor solid.

Properties of holes :

- It is missing electron in valence band.
- It's effective mass is more than electron.
- It acts as positive charge carrier.
- It's mobility is less than electron.

Hole acts as virtual charge, although there is no physical charge on it.

EFFECT OF IMPURITY IN SEMICONDUCTOR

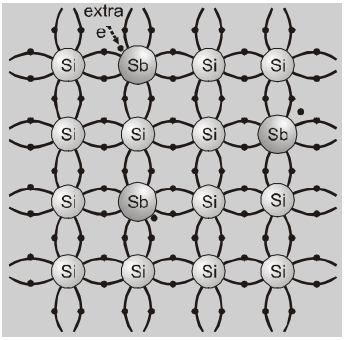
Doping is a method of addition of "desirable" impurity atoms to pure semiconductor to increase their conductivity.

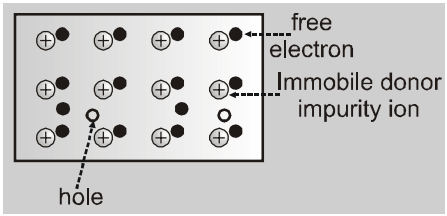
CLASSIFICATION OF SEMICONDUCTOR

Intrinsic semiconductor	Extrinsic semiconductor (Doped semicondutor)	
	N-type	P-type
(pure form of Ge, Si) $n_e = n_h = n_i$	pentavalent impurity (P, As, Sb) donor impurity (N_D) $n_e >> n_h$	trivalent impurity (B, In, Al) acceptor impurity (N_A) $n_h >> n_e$

N-type semiconductor

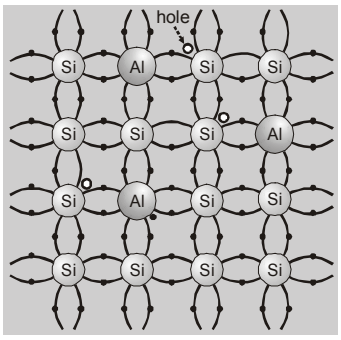
When a pure semiconductor (Si or Ge) is doped by pentavalent impurity (P, As, Sb) then four electrons out of the five valence electrons of impurity take part in covalent bonding, with four silicon atoms surrounding it and the fifth electron is set free. These impurity atoms which donate free e^- for conduction are called as Donor impurity (N_D). Here free e^- increases very much so it is called as "N" type semiconductor. Here impurity ions known as "Immobile Donor positive Ion". "Free e^-"called as "majority" charge carriers and "holes" called as "minority" charge carriers.

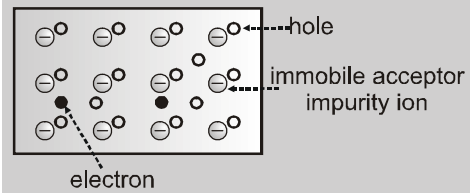


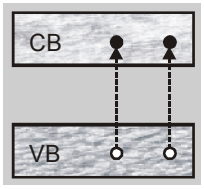
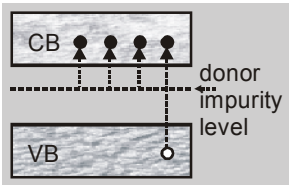
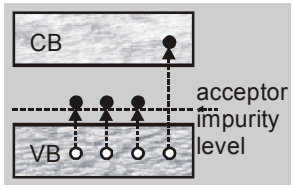
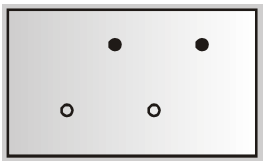
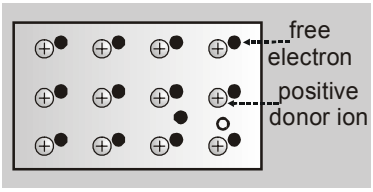
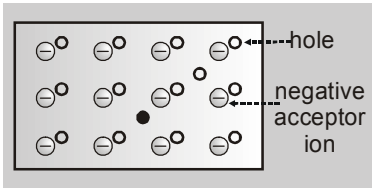


P-type semiconductor

When a pure semiconductor (Si or Ge) is doped by trivalent impurity (B, Al, In) then the outermost three electrons of the valence band of impurity, take part in covalent bonding with four silicon atoms surrounded by it. This shows that there remains a vacancy in the band. To fill this vacancy, an electron is accepted from the neighbouring atom leaving a hole from its own site. Thus an extra hole is formed. These impurity atoms accepting bonded e^- from valence band are called as Acceptor impurity (N_A). Here holes increases very much so it is called as "P" type semiconductor. Here impurity ions known as "Immobile Acceptor negative Ion". Free e^- are called as minority charge carries and holes are called as majority charge carriers.





	Intrinsic Semiconductor	N-type (Pentavalent impurity)	P-type(Trivalent impurity)
1.			
2.			
3.	Current is due to both electrons and holes	Mainly due to electrons	Mainly due to holes
4.	$n_e = n_h = n_i$	$n_e >> n_h$ ($N_D \simeq n_e$)	$n_h >> n_e$ ($N_A \simeq n_h$)
5.	$I = I_e + I_h$	$I \simeq I_e$	$I \simeq I_h$
6.	Entirely neutral	Entirely neutral	Entirely neutral
7.	Quantity of electrons and holes are equal	Majority - Electrons Minority - Holes	Majority - Holes Minority - Electrons

MASS ACTION LAW

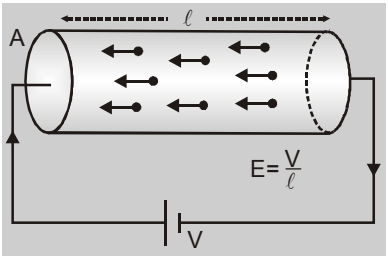
At room temperature, most of the acceptor atoms get ionised leaving holes in the valence band. Thus at room temperature the density of holes in the valence band is predominantly due to impurity in the extrinsic semiconductor. The electron and hole concentration in a semiconductor in thermal equilibrium is given by

$$n_e n_h = n_i^2$$

Though the above description is grossly approximate and hypothetical, it helps in understanding the difference between metals, insulators and semiconductors (extrinsic and intrinsic) in a simple manner.

RESISTIVITY AND CONDUCTIVITY OF SEMICONDUCTOR

- **Conduction in conductor**



As we know that the relation between current (I) and drift velocity (v_d) is

$I = neAv_d$ where n = number of electron in per unit volume

current density $J = \frac{I}{A} = nev_d$ ($\because$ drift velocity of electron $v_d = \mu E$)

$\therefore$ $J = ne\mu E = \sigma E$

$\therefore$ Conductivity $\sigma = ne\mu = 1/\rho$

and Resistivity $\rho = \frac{1}{ne\mu}$

- **Conduction in Semiconductor**

Intrinsic semiconductor	P - type	N - type
$n_e = n_h$	$n_h >> n_e$	$n_e >> n_h$
$J = ne [v_e + v_h]$	$J \cong e n_h v_h$	$J \cong e n_e v_e$
$\sigma = \frac{1}{\rho} = en[\mu_e + \mu_h]$	$\sigma = \frac{1}{\rho} \cong en_h\mu_h$	$\sigma = \frac{1}{\rho} \cong en_e\mu_e$

GOLDEN KEY POINTS

- Number of electrons reaching from valence band to conduction band at temperature T is given by

  $$n = A T^{3/2} e^{-\frac{\Delta Eg}{2kT}}$$

  where k = Boltzmann constant = 1.38×10^{-23} J/K , T = absolute temperature, A = constant

  ΔE_g = energy gap between conduction band and valence band
- In silicon at room temperature out of 10^{12} Si atoms only one electron goes from valence band to conduction band.
- In germanium at room temperature out of 10^9 Ge atoms only one electron goes from valence band to conduction band.
- In semiconductors, Ohms law is approximately obeyed only for low electric field (less than 10^6 Vm^{-1}). Above this field, the current becomes almost independent of applied field.
- The size of dopant (impurity atom) should be almost the same as that of crystal atom. So that crystalline structure of solid remain unchanged.
- Because of doping semiconducting lattice should not be disturbed therefore doping concentration is kept low. The doping ratio varies from

  impure : pure :: 1 : 10^6 to 1 : 10^{10}. In general it is 1 : 10^8
- Due to impurity the conductivity increases approximately 10^5 times.

Illustrations

Illustration 1.

A P type semiconductor has acceptor level 57 meV above the valence band. What is maximum wavelength of light required to create a hole ?

Solution

$$E = \frac{hc}{\lambda} \quad \Rightarrow \quad \lambda = \frac{hc}{E} = \frac{6.62\times10^{-34}\times3\times10^{8}}{57\times10^{-3}\times1.6\times10^{-19}} = 217700 \text{ Å}$$

Illustration 2.

A silicon specimen is made into a p-type semiconductor by doping on an average one indium atom per 5×10^7 silicon atoms. If the number density of atoms in the silicon specimen is 5×10^{28} atoms/m^3; find the number of acceptor atoms in silicon per cubic centimeter.

Solution

The doping of one indium atom in silicon semiconductor will produce one acceptor atom in p-type semiconductor. Since one indium atom has been dopped per 5×10^7 silicon atoms, so number density of acceptor atoms in

silicon $= \frac{5\times10^{28}}{5\times10^{7}} = 10^{21}$ atom/m^3 = = 10^{15} atoms/cm^3

Illustration 3.

Pure Si at 300 K has equal electron (n_e) and hole (n_h) concentrations of 1.5×10^{16} m^{-3}. Dopping by indium n_h increases to 3×10^{22} m^{-3}. Calculate n_e in the doped Si.

Solution

For a doped semi-conductor in thermal equilibrium $n_e n_h = n_i^2$ (Law of mass action)

$$n_e = \frac{n_i^2}{n_h} = \frac{(1.5\times10^{16})^2}{3\times10^{22}} = 7.5 \times 10^{9}\ m^{-3}$$

Illustration 4.

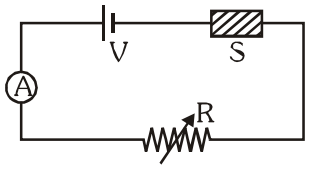
What will be conductivity of pure silicon crystal at 300 K temperature. If electron hole pairs per cm^3 is 1.072×10^{10} at this temperature, $\mu_e = 1350\ cm^2$ / volt-s & $\mu_h = 480\ cm^2$ / volt-s

Solution

$\sigma = n_i e\mu_e + n_i e\mu_h = n_i e(\mu_e + \mu_h) = 1.072 \times 10^{10} \times 1.6 \times 10^{-19} \times (1350 + 480) = 3.14 \times 10^{-6}$ mho/cm

BEGINNER'S BOX-1

1. The diagram shows a piece of pure semiconductor S, in series with a variable resistor R, and a source of constant voltage V. Would you increase or decrease the value of R to keep the reading of ammeter (A) constant, when semiconductor S is heated ? Give reason.



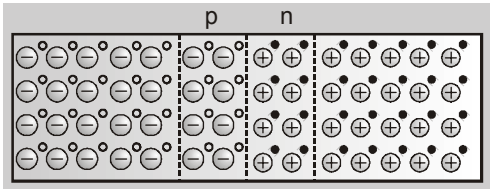
2. Pure Si at 300 K has equal electron n_e and hole n_h concentration of $1.5 \times 10^{16}/m^3$. Doping by indium increases n_h to $4.5 \times 10^{22}/m^3$. Calculate n_e in doped silicon.

3. Suppose a pure Si crystal has 5×10^{28} atoms m^{-3}. It is doped by 1 ppm concentration of pentavalent As. Calculate the number of electrons and hole. (Given that $n_i = 1{\cdot}5 \times 10^{16}\ m^{-3}$.)

4. For given semiconductor contribution of current due to electron and hole is in ratio 3/1 and the ratio of drift velocity for electron and hole is 5/2, then calculate the ratio of electron to hole concentration.

P-N JUNCTION

Given diagram shows a P–N junction immediately after it is formed.

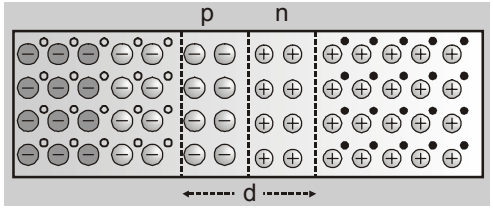


P region has mobile majority holes and immobile negatively charged impurity ions.

N region has mobile majority free electrons and immobile positively charged impurity ions.

Due to concentration difference diffusion of holes starts from P to N side and diffusion of e^- s starts from N to P side.

Due to this a layer of only positive ions (in N side) and negative ions (in P–side) started to form which generate an electric field (N to P side) which oppose diffusion process, during diffusion magnitude of electric field increases due to this diffusion it gradually decreased.



The layer of immobile positive and negative ions, which have no free electrons and holes called as **depletion layer** as shown in diagram.

Due to internal electrical field, an electron on p-side of the junction moves to n-side and a hole on n-side of the junction moves to p-side. The motion of charge carriers due to the electric field is called drift. Thus a drift current flows, which is opposite in direction to the diffusion current.

Initially, diffusion current is large and drift current is small. As the diffusion process continues, the space-charge regions on either side of the junction extend, thus increasing the electric field strength and hence drift current. This process continues until the diffusion current equals the drift current.

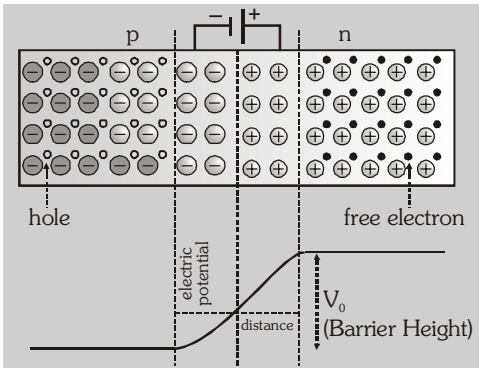
At equilibrium condition

Direction of diffusion current : P to N side and drift current : N to P side

If there is no biasing then | diffusion current | = | drift current |

So total current is zero.

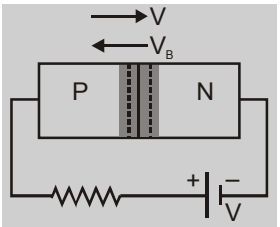
In junction N side is at high potential relative to the P side. This potential difference tends to prevent the movement of electron from the N region into the P region. This potential difference is called **Barrier potential**.



BEHAVIOUR OF P–N JUNCTION WITH AN EXTERNAL VOLTAGE APPLIED OR BIAS

- **Forward Bias**

In this type of biasing we apply a potential difference such that P–side is at high potential and N–side is at low potential as shown in the diagram.

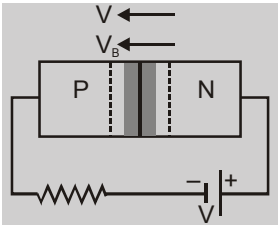


The applied voltage is opposite to the junction barrier potential.

Due to this effective potential barrier decreases, junction width also decreases, so more majority carriers will be allowed to flow across junction. It means the current flow in principally due to majority charge carries called as forward current (in mA).

- **Reverse Bias**

In this type of biasing we apply a potential difference such that P–side is at low potential and N–side is at high potential as shown in the diagram.



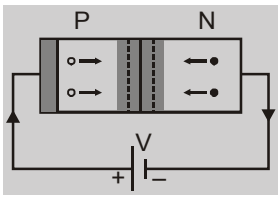
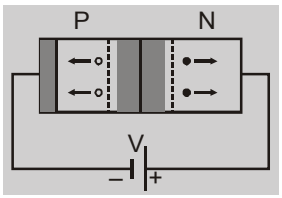
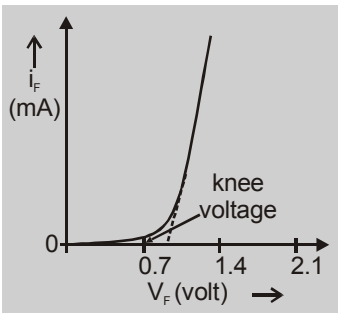
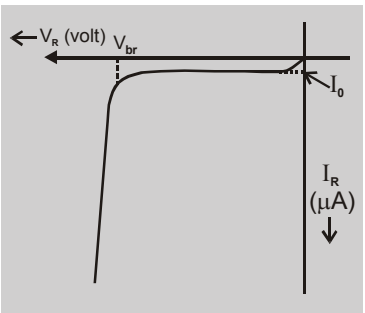
The applied voltage is same side of to the junction barrier potential. Due to this effective potential barrier increased, junction width also increased, so no majority carriers will be allowed to flow across junction.

Only minority carriers are drifted. It means the current flow in principally due to minority charge carries and is very small (μA) called as reverse current.

The current under reverse bias is essentially voltage independent upto a critical reverse bias voltage, known as breakdown voltage (V_{br}). When $V = V_{br}$, the diode reverse current increases sharply. Even a slight increase in the bias voltage causes large change in the current. This phenomena is known as **Breakdown**.

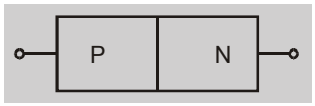
Breakdown are of two types :-

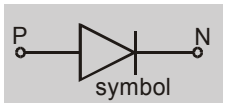
Zener Breakdown	Avalanche Breakdown
• Where covalent bonds of depletion layer, itself break, due to high electric field of very high Reverse bias voltage. • This phenomena takes place in (i) P – N junction having "High doping" (ii) P – N junction having thin depletion layer • Here P – N junction does not damage permanently "In D.C voltage stablizer zener phenomena is used".	• Here covalent bonds of depletion layer are broken by collision of "Minorities" which aquire high kinetic energy from high electric field of very-very high reverse bias voltage. • This phenomena takes place in (i) P – N junction having "Low doping" (ii) P – N junction having thick depletion layer • Here P – N junction damages permanently due to abruptly increment of minorities during repeatative collisions.

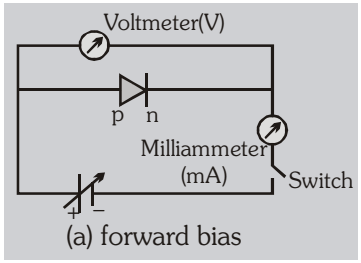
	Forward Bias		**Reverse Bias**
	P → positive N → negative 		P → negative N → positive 
1.	Potential Barrier reduces.	1.	Potential Barrier increases.
2.	Width of depletion layer decreases.	2.	Width of depletion layer increases.
3.	P-N Junction provides very small resistance.	3.	P-N Junction provides high resistance.
4	Forward current flow in circuit.	4.	Reverse current flow in circuit.
5.	Order of forward current is milli ampere.	5.	Order of current is micro ampere (Ge) or Nano ampere (Si).
6.	Mainly majority current flows.	6.	Mainly minority current flows.
7.	Forward characteristic curve 	7.	Reverse characteristic curve 
8.	Forward resistance $R_f = \frac{\Delta V_f}{\Delta I_f} \cong 100\Omega$	8.	Reverse resistance $R_B = \frac{\Delta V_B}{\Delta I_B} \cong 10^6\Omega$

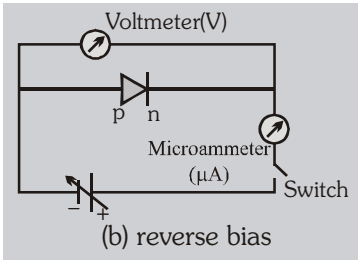
9. Knee or cut in voltage Ge → 0.3 V , Si → 0.7 V	9. Breakdown voltage Ge → 25 V, Si → 35 V
10. Forward current Equation $I = I_o\left[e^{+\frac{qV}{kt}} - 1\right]$ $\because \quad e^{\frac{qv}{kt}} >> 1$ $\therefore \quad I \cong I_o e^{\frac{qv}{kt}}$ (exp. increment) For Ge $\frac{R_B}{R_F} = 10^3 : 1$	10. Reverse current equation $I = I_0\left[e^{-\frac{qV}{KT}} - 1\right]$ $\because \quad e^{-\frac{qv}{KT}} << 1$ $\therefore \quad I \simeq -I_0$ For Si $\frac{R_B}{R_F} = 10^4 : 1$

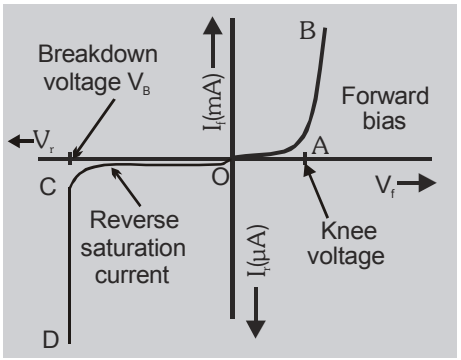
Characteristic Curve of P-N Junction Diode







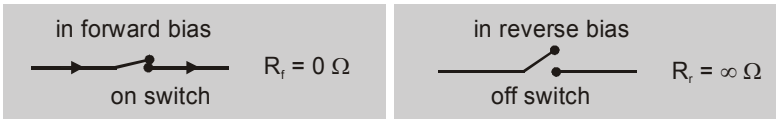




In forward bias when voltage is increased from 0V in steps and corresponding value of current is measured, the curve comes as OB of figure. We may note that current increases very sharply after a certain voltage knee voltage. At this voltage, barrier potential is completely eliminated and diode offers a low resistance.

In reverse bias a microammeter has been used as current is very very small. When reverse voltage is increased from 0V and corresponding values of current measured the plot comes as OCD. We may note that reverse current is almost constant hence called reverse saturation current. It implies that diode resistance is very high. As reverse voltage reaches value V_B, called breakdown voltage, current increases very sharply.

For Ideal Diode



GOLDEN KEY POINTS

- Width of depletion layer $\cong$ 0.1 μm

  (a) As doping increases, width of depletion layer decreases

  (b) P-N junction $\rightarrow$ nonohmic, due to nonlinear relation between I and V.

- Potential Barrier or contact potential for Ge $\rightarrow$ 0.3 V, for Si $\rightarrow$ 0.7 V

- Strength of junction field $E = \frac{\Delta V}{d} = \frac{0.5}{10^{-7}} \Rightarrow E \cong 10^6$ V/m

  This field prevents the respective majority carriers from crossing barrier region.

- In reverse bias, the current is very small and nearly constant with bias (termed as reverse saturation current). However interesting behaviour results in some special cases if the reverse bias is increased further beyond a certain limit, breakdown of depletion layer takes place.

Illustrations

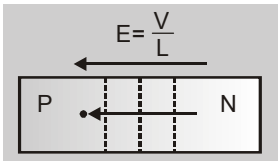
Illustration 5.

A potential barrier of 0.5 V exists across a p-n junction (i) If the depletion region is 5×10^{-7} m wide. What is the average intensity of the electric field in this region ? (ii) An electron with speed 5×10^5 m/s approaches the p-n junction from the n-side with what speed will it enter the p-side?

Solution:

(i) Width of depletion layer $\Delta L = 5 \times 10^{-7}$ m

$$E = \frac{V}{\Delta L} = \frac{0.5V}{5 \times 10^{-7}} = 10^6 \text{ volt/m}$$



(ii) Work energy theorem $\frac{1}{2}Mv_i^2 = eV + \frac{1}{2}Mv_f^2$

$$v_f = \sqrt{\frac{Mv_i^2 - 2eV}{M}} = 2.7 \times 10^5 \text{ m/s}$$

Illustration 6.

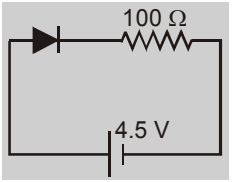
Figure shows a diode connected to an external resistance and an e.m.f. Assuming that the barrier potential developed in diode is 0.5 V, obtain the value of current in the circuit in milliampere.

Solution

E = 4.5 V, R = 100 Ω,

voltage drop across p-n junction = 0.5 V

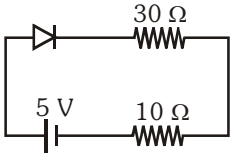
effective voltage in the circuit V = 4.5 – 0.5 = 4.0 V



current in the circuit $I = \frac{V}{R} = \frac{4.0}{100} = 0.04$ A $= 0.04 \times 1000$ mA $= 40$ mA

Illustration 7.

If current in given circuit is 0.1 A then calculate resistance of P–N junction.

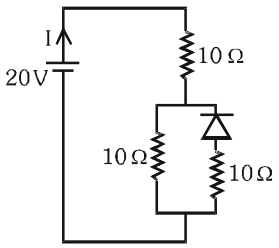


Solution

Let resistance of PN junction be R then $I = \frac{5}{R + 30 + 10} = 0.1 \Rightarrow R = 10\ \Omega$

Illustration 8.

What is the value of current I in given circuits

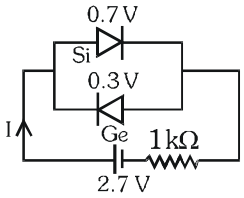


Solution

$$I = \frac{20}{10+10} = 1 \text{ A}$$

Illustration 9.

What is the value of current I in given circuits

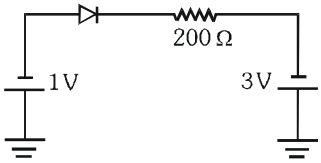


Solution

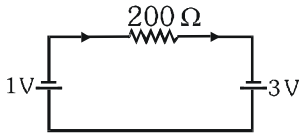
$$I = \frac{2.7-0.7}{1\times10^{3}} = 2 \text{ mA}$$

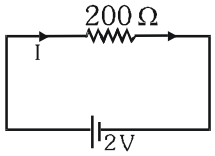
Illustration 10.

In the giving circuit. If P–N junction is ideal, then calculate current flowing through it.



Solution.

In given condition 

≡ 

$\Rightarrow I = \frac{2V}{200} = 0.01$ A

BEGINNER'S BOX-2

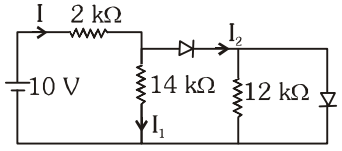
1. The potential barrier existing across an unbiased p–n junction is 0.2 volt. What minimum kinetic energy a hole should have to diffuse from the p–side to the n–side if –

(a) The junction is unbiased (b) The junction is forward biased at 0.1 volt

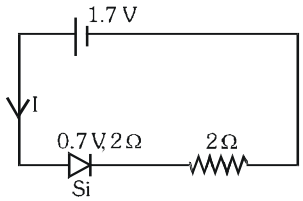
(c) The junction is reverse–biased at 0.1 volt.

2. A silicon P–N junction is in forward biased condition with a resistance in series. It has knee voltage of 0.75 V and current flow in it is 10 mA. If the P–N junction is connected with 2.75 V battery then calculate the value of the resistance.

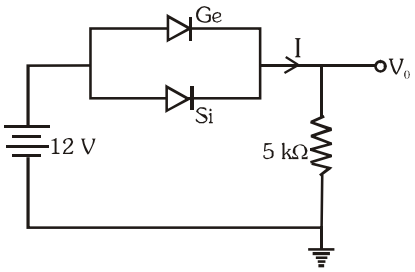
3. In given circuit determine I, I_1 and I_2



4. Find the value of current I in given circuit.



5. (a) Calculate the value of V_0 and I if the Si diode and the Ge diode start conducting at 0·7 V and 0·3 V respectively, in the given circuit. (b) If the Ge diode connection be reversed, What will be the new values of V_0 and I ?



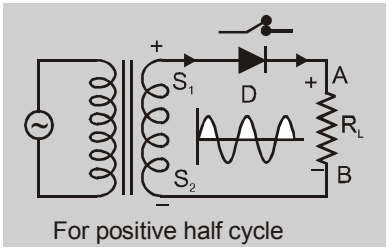
APPLICATION OF JUNCTION DIODE :

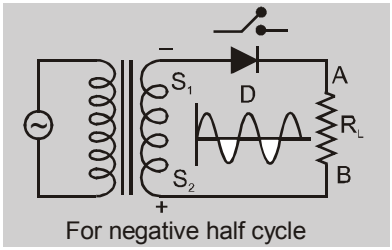
Rectifier

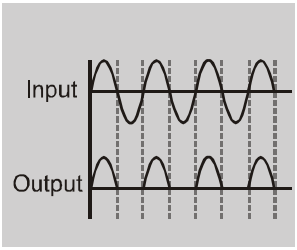
It is device which is used for converting alternating current into direct current.

(i) Half wave rectifier

It rectifies only half of the ac input wave.







During the first half (positive) of the input signal, S_1 is at positive and S_2 is at negative potential. So, the PN junction diode D is forward biased. The current flows through the load resistance R_L and output voltage is obtained across the R_L.

During the second half (negative) of the input signal, S_1 is at negative potential and S_2 is at positive potential. The PN junction diode will be reversed biased. In this case, practically no current would flow through the load resistance. So, there will be no output across the R_L.

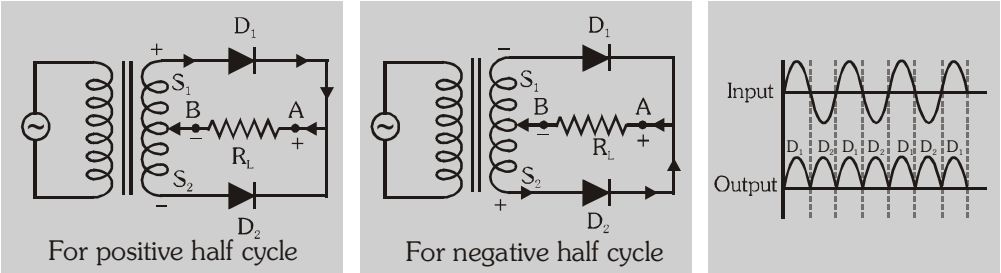
Thus, corresponding to an alternating input signal, we get a unidirectional pulsating output called rectified output.

2. Full wave rectifier

It rectifies both the cycles of input ac wave. It is of two types (fundamentally).

(i) Centre tap rectifier

Figure shows the experiemental arrangement for using diode as full wave rectifier. When the alternating signal is fed to the transformer, the output signal appears across the load resistance R_L.

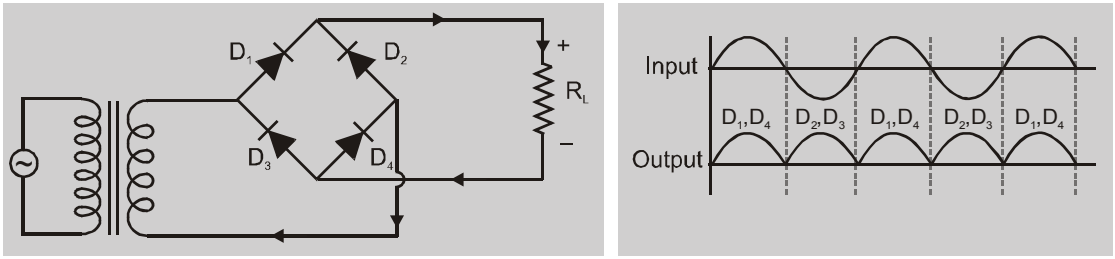


During the positive half of the input signal : S_1 positive and S_2 negative. In this case diode D_1 is forward biased and D_2 is reverse biased. So only D_1 conducts and hence the flow of current in the load resistance R_L is from A to B.

During the negative half of the input signal : S_1 is negative and S_2 is positive. So D_1 is reverse-biased and D_2 is forward biased. So only D_2 conducts and hence the current flows through the load resistance R_L again from A to B.

It is clear that whether the input signal is positive or negative, the current always flows through the load resistance in the same direction and thus output is called full wave rectified.

(ii) Bridge Rectifier



During positive half cycle

D_1 and D_4 are foward biased → 'On' switch

D_2 and D_3 are reverse biased → 'Off' switch

During negative half cycle

D_2 and D_3 are foward biased → 'On' switch

D_1 and D_4 are reverse biased → 'Off' switch

- **Rectifier efficiency (η)** $\eta\% = \dfrac{P_{dc}}{P_{ac}} = \dfrac{I_{dc}^2 R_L}{I_{rms}^2 (R_F + R_L)} \times 100$

For half wave rectifier

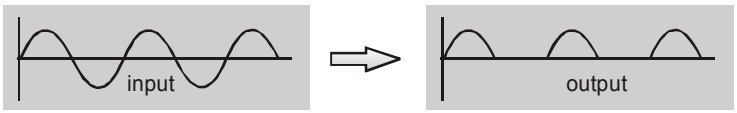
$\eta_{max} = 40.6\ \%$

For full wave rectifier or bridge wave rectifier

$\eta_{max} = 81.2\ \%$

- **Ripple Frequency**

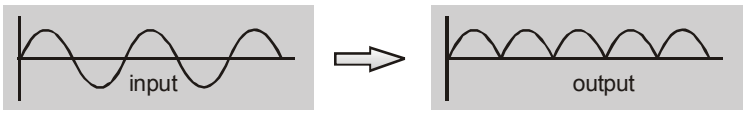
(i) For half wave rectifier



Input frequency = 50 Hz

Ripple frequency = 50 Hz

(ii) for full wave rectifier



Input frequency = 50 Hz

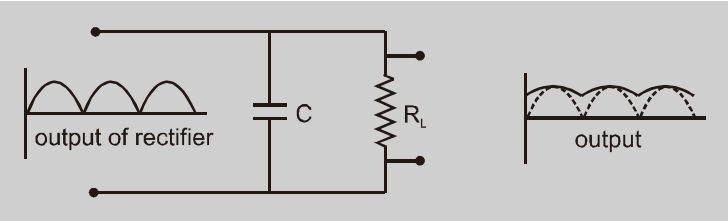
Ripple frequency = 100 Hz

Filter Circuit

The rectified output is in the form of pulses or in shape of half sinusoids. Though it is unidirectional, it does not have a steady value. To get steady dc output from the pulsating voltage, normally a capacitor is connected across the output terminals (parallel to the load R_L) called filter circuit.

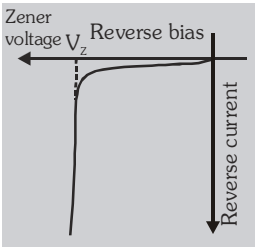
- **Capacitor Filter**

When the voltage across the capacitor is rising, it gets charge. If there is no external load, it remains charged to the peak voltage of the rectified output. When there is a load, it gets discharged through the load and the voltage across it begins to fall. In the next half-cycle of rectified output it again gets charged to the peak value but due to large value of time constant of capacitor, voltage across the capacitor approximate remains constant.



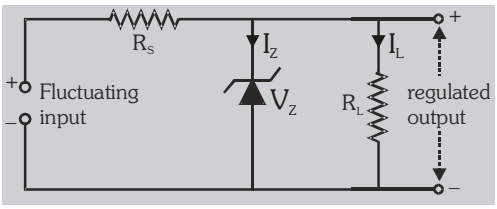
ZENER DIODE

It is a special purpose diode, designed to operate under the reverse bias in the breakdown region and used in voltage regulation. Symbol of Zener diode is 



In reverse bias of zener diode after the breakdown voltage V_Z, a large change in the current can be produced by almost insignificant change in the reverse bias voltage. In other words zener voltage remains constant, even through current through the zener diode varies over a wide range. This property of the zener diode is used for regulating voltage.

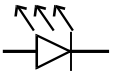
Zener diode as a voltage regulator



The unregulated dc voltage (filtered output of a rectifier) is connected to the zener diode through a series resistance R_S such that the zener diode is reverse biased. If the input voltage increases, the current through R_S and zener diode also increases. This increases the voltage drop across R_S without any change in the voltage across the zener diode. This is because in the breakdown region, zener voltage remains constant even though the current through the zener diode changes. Similarly, if the input voltage decreases, the current through R_S and zener diode also decreases. The voltage drop across R_S decreases without any change in the voltage across the zener diode. Thus any increase/decrease in the input voltage results in, increase/ decrease of the voltage drop across R_S without any change in voltage across the zener diode. Thus the zener diode acts as a voltage regulator.

OPTOELECTRONIC JUNCTION DEVICES

1. Light emitting diode (L.E.D)

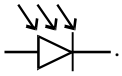
It is a heavily doped P-N junction which under forward bias emits spontaneous radiation. Its symbol is 

when LED is forward biased then electrons move from N → P and holes move from P → N. At the junction boundary these are recombined. On recombination, energy is released in the form of photons of energy equal to or slightly less than the band gap.

When the forward current of the diode is small, the intensity of light emitted is small. As the forward current increases, intensity of light increases and reaches a maximum. Further increase in the forward current results in decrease of light intensity. LEDs are biased in such a way that the light emitting efficiency should be maximum.

In case of Si or Ge diodes, the energy released in recombination lies in infra-red region. Therefore to form LED, such semiconductors are to be used which have band gap from 1.8 eV to 3 eV. Hence $GaAs_{1-x}P_x$ is used in forming LED.

2. Photodiode

It is a special purpose junction diode used to sense and measure incident light. its symbol is  .

It is operated under reverse bias.

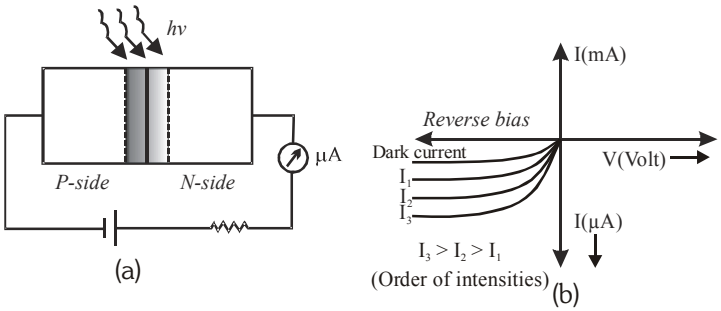
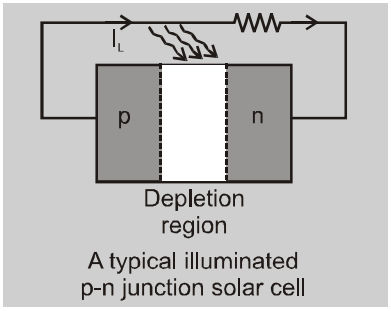


Figure (a) An illuminated photodiode, under reverse bias
(b) I-V characteristics of a photodiode for different illumination intensity
$I_3 > I_2 > I_1$

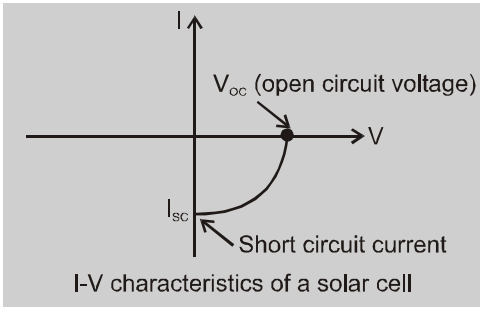
When light of energy "hν" falls on the photodiode (Here hν > energy gap) more electrons move from valence band to conduction band, due to this current in circuit of photodiode in "Reverse bias", increases. As light intensity is increased, the photo current goes on increasing. So photo diode is used "to detect light intensity". Example used in "Video camera".

3. Solar cell

A p-n junction which generates emf when solar radiation falls on it, called solar cell. It works on the same principle (photovoltaic effect) as the photodiode, except that no external bias is applied and the junction area is kept much larger for solar radiation to be incident because we are interested in more power.



(a)



(b)

When light falls on, emf generates due to the following three basic processes: generation, separation and collection- (i) generation of e-h pairs due to light (with hν > Eg) in junction region; (ii) separation of electrons and holes due to electric field of the depletion region. Electrons are swept to n-side and holes to p-side by the junction field; (iii) On reaching electrons at n-side and holes on at p-side. Thus n-side becomes negative and p-side becomes positive potential and giving rise to photovoltage.

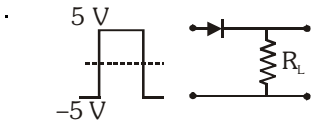
GOLDEN KEY POINTS

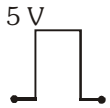
- RMS and average (dc) current for Half wave rectifier $I_{rms} = \frac{I_0}{2}$, $I_{dc} = \frac{I_0}{\pi}$ for Full wave rectifier $I_{rms} = \frac{I_0}{\sqrt{2}}$, $I_{dc} = \frac{2I_0}{\pi}$
- Maximum efficiency of half wave rectifier is 40.6% and of full wave rectifier is 81.2%
- Ripple and ripple factor (r) : In the output of rectifier some A.C. components are present, these are called ripples & their measurement is given by a factor called ripple factor. For good rectifier ripple factor must be very low.
  for HWR r = 1.21, for FWR r = 0.48
- Dark current : When no light is incident then the reverse saturation current in photo diode is called dark current.
- LED have less power and low operating voltage.
- Solar cell converts solar energy into electrical energy.
- Zener diode is heavily doped with thin depletion region.

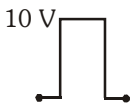
Illustrations

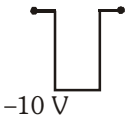
Illustration 11.

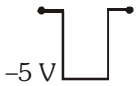
If in a p-n junction diode, a square input signal of 10 V is applied as shown. Then, the output signal across R_L will be :- **[AIEEE - 2007]**



(1) 

(2) 

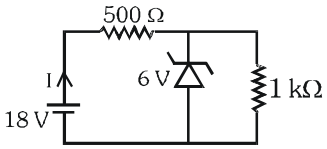
(3) 

(4) 

Solution **Ans. (1)**

Illustration 12.

What is the value of current I in given circuits?



Solution

$$I = \frac{18-6}{500} = 24 \text{ mA}$$

Illustration 13.

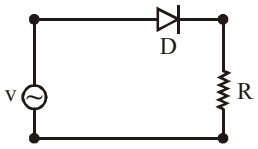
A photodetector is made from a semiconductor with E_g= 0.75 eV. Calculate the maximum wavelength which it can detect ?

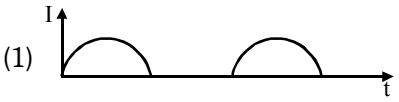
Solution :

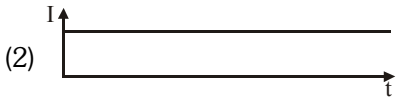
$$\lambda_{max} = \frac{hc}{E_g} = \frac{6.62\times10^{-34}\times3\times10^{8}}{0.75\times1.6\times10^{-19}} = 16553 \text{ Å}$$

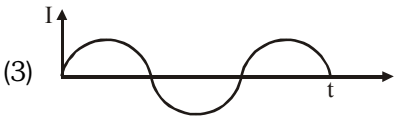
BEGINNER'S BOX-3

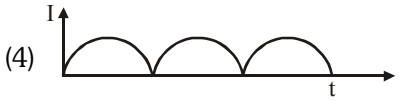
1. A p-n junction diode (D) shown in the figure can act as a rectifier. An alternating current source (V) is connected in the circuit. The current (I) in the resistor (R) can be shown by :- **[AIEEE - 2009]**











2. A zener diode of voltage V_Z (=6 V) is used to maintain a constant voltage across a load resistance R_L (=1000 Ω) by using a series resistance R_S (=100 Ω). If the e.m.f. of source is E (= 9 V), calculate the value of current through series resistance, Zener diode and load resistance. What is the power being dissipated in Zener diode?

3. A Zener diode is specified having a breakdown voltage of 9.1 V with a maximum power dissipation of 364 mW. What is the maximum current that the diode can handle?

4. A semiconductor (GaAs) has an energy gap of 1.43 eV. What is the maximum wavelength emitted when a hole and an electron recombine in such semiconductor?

TRANSISTOR

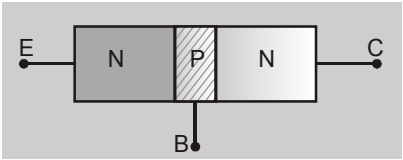
Transistor is a three terminal device which transfers a singal from low resistance circuit to high resistance circuit.

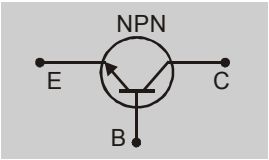
It is formed when a thin layer of one type of extrinsic semiconductor (P or N type) is sandwitched between two thick layers of other type of extrinsic semiconductor.

Transistors are of two types

- **N-P-N Transistor**

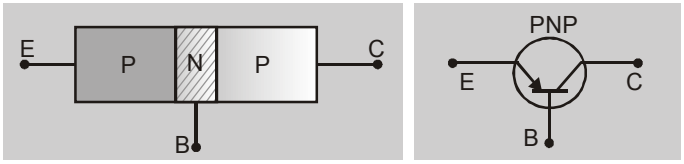
If a thin layer of P-type semiconductor is sandwitched between two thick layers of N-type semiconductor, then it is known as NPN transistor.





- **P-N-P Transistor**

If a thin layer of N-type of semiconductor is sandwitched between two thick layer of P-type semiconductor, then it is known as PNP transistor.



Each transistor has three terminals and these are :-

(i) Emitter

It is the left most part of the transistor which emits the majority carriers towards base. It is **highly doped** and **medium in size**.

(ii) Base

It is the middle part of transistor which is sandwitched by emitter (E) and collector (C). It is **lightly doped** and **very thin in size**.

(iii) Collector

It is right part of the transistor which collects the majority carriers which is emitted by emitter. It has **large size** and **moderate doping**.

Every transistor has following two junctions

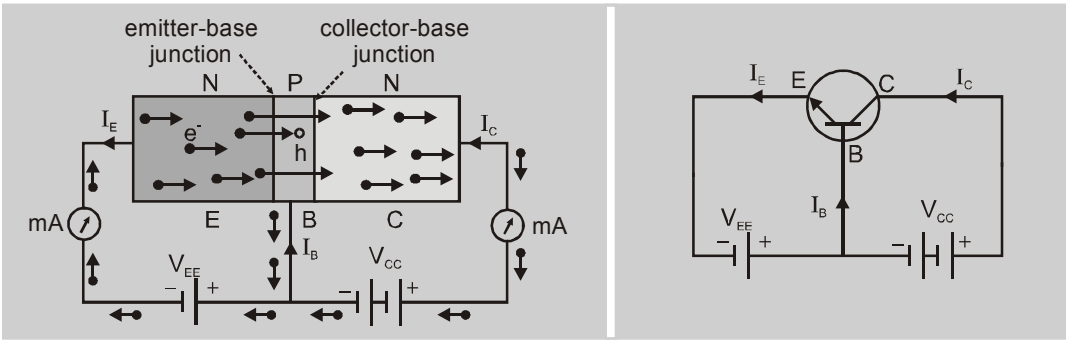
(i) The junction between emitter and base is known as emitter-base junction **(J_{EB})**.

(ii) The junction between base and collecter is known as base-collector junction **(J_{BC})**.

WORKING OF TRANSISTOR

1. Working of NPN Transistor

The emitter base junction is forward biased and base collector junction is reversed biased to study the behaviour of transistor. It is called active state of transistor. N-P-N transistor in circuit and symbolic representation is shown in figure.



In active state of n-p-n transistor majority electrons in emitter are sent towards base.

The barrier of emitter base junction is reduced because of forward bias therefore electrons enter into the base. About 5% of these electrons recombine with holes in base region results very small current (I_B) in base.

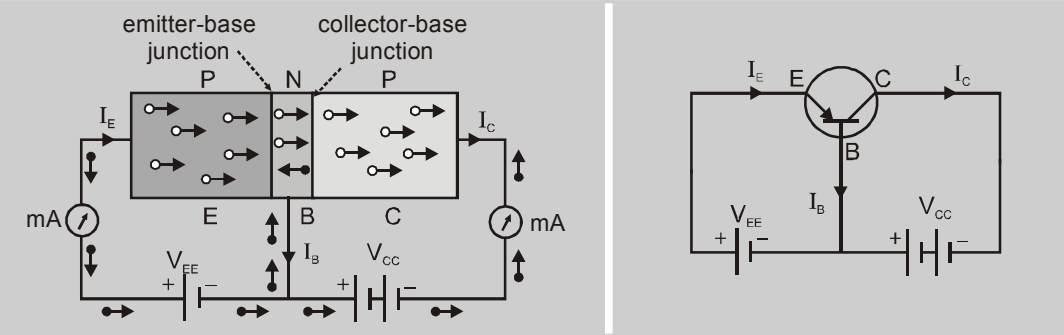
The remaining electron ($\approx 95\%$) enters into the collector region because these are attracted towards the positive terminal of battery results collecter current (I_C)

The base current is the difference between I_E and I_C and proportional to the number of electron hole recombination in the base.

$I_E = I_B + I_C$, We also see $I_E \simeq I_C$ because I_B is very small.

2. Working of PNP Transistor

When emitter-base junction is forward biased, holes (majority carriers) in the emitter are repelled towards the base and diffuse through the emitter base junction. The barrier potential of emitter-base junction decreases and hole enters into the n-region (i.e. base). A small number of holes ($\approx 5\%$) combine with electrons of base-region resulting small current (I_B). The remaining holes ($\approx 95\%$) enter into the collector region because these are attracted towards negative terminal of the battery connected with the collector-base junction. These hole constitute the collector current (I_C).



As one hole reaches the collector, it is neutralized by the battery. As soon as one electron and a hole is neutralized in collector, a covalent bond is broken in emitter region and an electron hole pair is produced. The released electron enters the positive terminal of battery and holes moves towards the collector. So $I_E = I_B + I_C$

CONFIGURATIONS OF A TRANSISTOR AND ITS CHARACTERISTICS

The transistor is connected in either of the three ways in circuit.

(i) Common base configuration (ii) Common emitter configuration (iii) Common collector configuration

In these three, common emitter is widely used and common collector is rarely used.

- **Common emitter transistor characteristics**

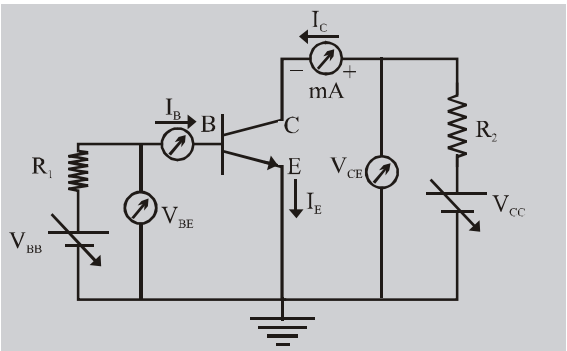


Figure : Circuit diagram for characteristics curve of n-p-n transistor (CE)

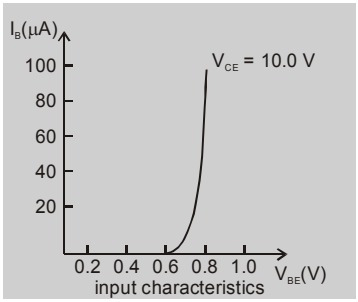
- **Input characterstics**

The variation of base current (I_B) (input) with base emitter voltage (V_{EB}) at constant collector emitter voltage (V_{CE}) is called input characteristic.

(i) Keep the collector-emitter voltage (V_{CE}) constant (say V_{CE} = 10 V)

(ii) Now change emitter base voltage V_{BE} in steps of 0.1 volt and note the corresponding values of base current (I_B).

(iii) Plot the graph between V_{BE} and I_B.



- **Output characteristics**

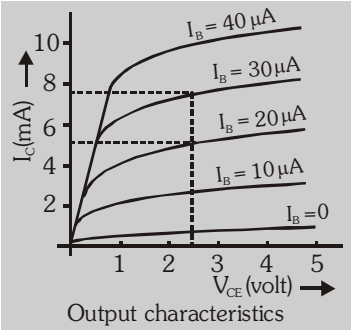
The variation of collector current I_C (output) with collector-emitter voltage (V_{CE}) at constant base current (I_B) is called output characteristic.

(i) Keep the base current (I_B) constant (say I_B = 10 μA)

(ii) Now change the collector-emitter voltage (V_{CE}) and note the corresponding values of collector current (I_C).

(iii) Plot the graph between V_{CE} and I_C.

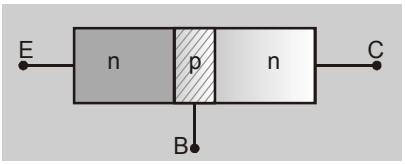
(iv) A set of such curves can also be plotted at different fixed values of base current (say 20 μA, 30 μA etc.)



Output characteristics

GOLDEN KEY POINTS

Emitter	Medium size	High doping
Base	Smallest size	Low doping
Collector	Largest size	Medium doping



- Transistor have two P-N Junction J_{EB} and J_{CB}. On the basis of junction condition transistor work in four regions.

Emitter-Base	Collector-Base	Region of working
Forward biased	Reverse biased	Active
Reverse biased	Forward biased	Inverse active
Reverse biased	Reverse biased	Cut off
Forward biased	Forward biased	Saturation

- The collector region is made physically larger than the emitter. Because collector has to dissipiate much greater power.
- Transistor mostly works in active region in electronic devices to use as an amplifier.
- Transistor i.e. It is a short form of two words "Transfer resistors". Signal is introduced at low resistance circuit and output is taken at high resistance circuit.
- Base is lightly doped, otherwise the most of the charge carries from the emitter recombine in base region and none of the emitted carrier reaches at collector.
- Transistor is a current operated device i.e. the action of transistor is controlled by the motion of charge carriers.
- From transistors characteristics,

(i) Input resistance $r_{in} = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE}\ =\ \text{constant}}$

(ii) Output resistance $r_{out} = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B\ =\ \text{constant}}$

(iii) Current gain $\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}\ =\ \text{constant}}$

- The ratio of change in output current to change in input voltage is known as transconductance.

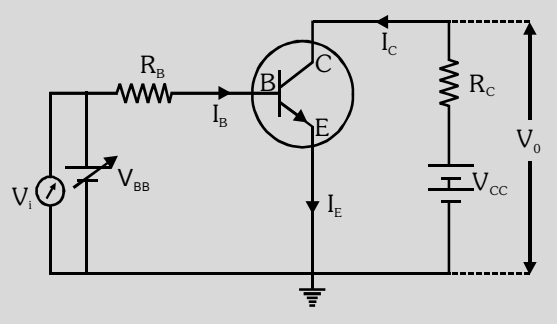
In CE transistor transconductance $(g_m) = \frac{\Delta I_C}{\Delta V_{in}}$.

- Voltage gain $A_V = \frac{\Delta V_o}{\Delta V_{in}} = \frac{(\Delta I_C)R_C}{\Delta V_{in}} = g_m \times R_C$

APPLICATIONS OF TRANSISTOR

1. Transistor as a switch

When a transistor is used in the cut off (off state) or saturation state (on state) only, it acts as a switch. To study this behaviour, we understand base biased CE transistor circuit.

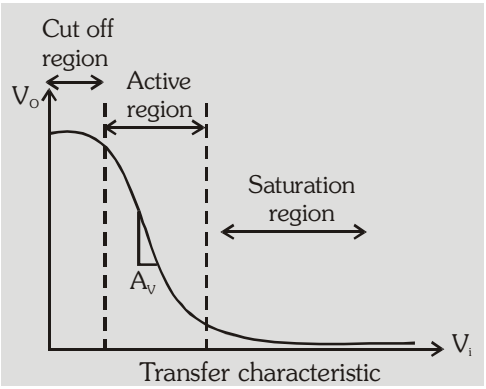


Applying Kirchhoff's voltage rule to the input and output sides of this circuit we get

$$V_i = I_B R_B + V_{BE} \quad (V_i = \text{dc input voltage})$$

and $$V_O = V_{CC} - I_C R_C \quad (V_O = \text{dc output voltage})$$

Now we can analyse how V_O changes as V_i increase from zero onwards. In case of Silicon transistor, if V_i is less than 0.6 V, I_B will be zero, hence I_C will zero and transistor will be said to be in cut-off state, and $V_O = V_{CC}$. When V_i become greater than 0.6 V, some I_B flows, so some I_C flows (transistor is in active state now) and output V_O decreases as the term $I_C R_C$ increase. With increase in V_i the I_C increase almost linearly and so V_O decreases linearly till its value becomes less than about 1.0 volt.



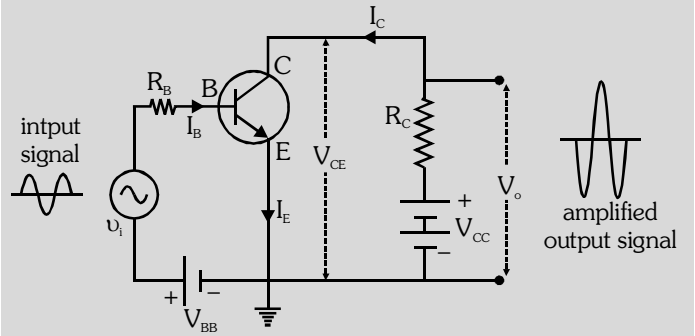
Beyond this, the change becomes non linear and transistor goes into saturation state. With further increase in V_i the output voltage is found to decrease further forwards zero (however, it may never become zero).

If we draw the V_O versus V_i curve called transfer characteristic (see figure), we see that between cut off state and active state and also between active state and saturation state there are regions of non-linearity showing that the transition from cut-off state to active state and from active state to saturation state are not sharply defined.

2. Transistor as an amplifier

The process of increasing the amplitude of input signal without distorting its wave shape and without changing its frequency is known as amplification.

A device which increases the amplitude of the input signal is called amplifier.



common emitter amplifier NPN transistor

To operate the transistor as an amplifier it is necessary to fix its operating point somewhere in the middle of its active region. If we fix the value of V_{BB} corresponding to a point in the middle of the linear part of the transfer curve then the dc base current I_B would be constant and corresponding collector current I_C will also be constant. The dc voltage $V_{CE} = V_{CC} - I_C R_C$ would also remain constant. The operating values of V_{CE} and I_B determine the operating point, of the amplifier.

If a small sinusoidal voltage with amplitude υ_i is superposed in series with the V_{BB} supply, then the base current will have sinusoidal variations superimposed on the value of I_B. As a consequence the collector current also will have sinusoidal variations superimposed on the value of I_C producing in turn corresponding change in the value of V_o.

Mathematical Analysis :

From KVL equation of base biased CE transistor circuit

$$V_i = I_B R_B + V_{BE}$$

$$\Rightarrow \quad \Delta V_i = (\Delta I_B)R_B + \Delta V_{BE} \qquad \because \Delta V_{BE} = 0 \qquad \Rightarrow \quad \Delta V_i = (\Delta I_B)\, R_B$$

Similarily $V_o = V_{CC} - I_C R_C$

$$\Rightarrow \quad \Delta V_o = \Delta V_{CC} - (\Delta I_C)R_C \qquad \because \Delta V_{CC} = 0 \qquad \Rightarrow \quad \Delta V_o = -(\Delta I_C)R_C$$

So voltage gain of CE amplifier

$$A_V = \frac{\Delta V_o}{\Delta V_{in}} = \frac{-(\Delta I_C)R_C}{(\Delta I_B)R_B} = -\beta \frac{R_C}{R_B}$$

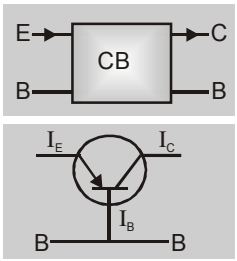
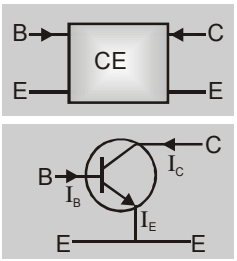
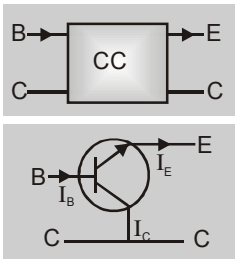
The negative sign represents that output voltage is opposite in phase with the input voltage.

Power gain (A_p) = current gain × voltage gain = $\beta_{ac} \times A_V \Rightarrow A_P > 1$

However it should be realised that transistor is not a power generating device. The energy for the higher ac power at the output is supplied by the battery V_{CC}.

Comparative study of transistor configuration

1. Common Base **(CB)** 2. Common Emitter **(CE)** 3. Common Collector **(CC)**

	C B	**C E**	**C C**
			
Input Resistance	Low (100 Ω)	High (750 Ω)	Very High ≅ 750 kΩ
Output resistance	Very High	High	Low
Current Gain	$(A_i$ or $\alpha)$ $\alpha = \frac{I_C}{I_E} < 1$	$(A_i$ or $\beta)$ $\beta = \frac{I_C}{I_B} > 1$	$(A_I$ or $\gamma)$ $\gamma = \frac{I_E}{I_B} > 1$
Voltage Gain	$A_V = \frac{V_o}{V_i} = \frac{I_C R_L}{I_E R_i}$ $A_v = \alpha \frac{R_L}{R_i}$	$A_V = \frac{V_o}{V_i} = \frac{I_C R_L}{I_B R_i}$ $A_v = \beta \frac{R_L}{R_i}$	$A_V = \frac{V_o}{V_i} = \frac{I_E R_L}{I_B R_i}$ $A_v = \gamma \frac{R_L}{R_i}$
Power Gain	$A_p = \frac{P_o}{P_i}$ $A_p = \alpha^2 \frac{R_L}{R_i}$	$A_p = \frac{P_o}{P_i}$ $A_p = \beta^2 \frac{R_L}{R_i}$	$A_p = \frac{P_o}{P_i}$ $A_p = \gamma^2 \frac{R_L}{R_i}$
Phase difference (between output and input)	same phase	opposite phase	same phase
Application	For High Frequency amplifier	For Audible frequency amplifier	For Impedance Matching

Relation between α, β and γ

α , β	β , γ	α , γ
$I_E = I_B + I_C$	$I_E = I_B + I_C$	$I_E = I_B + I_C$
divide by I_C	divide by I_B	$\because \gamma = 1 + \beta$
$\frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$	$\frac{I_E}{I_B} = 1 + \frac{I_C}{I_B}$	$\gamma = 1 + \frac{\alpha}{1-\alpha}$
$\frac{1}{\alpha} = \frac{1}{\beta} + 1$	$\gamma = 1 + \beta$	$\gamma = \frac{1}{1-\alpha}$
$\beta = \frac{\alpha}{1-\alpha}$, $\alpha = \frac{\beta}{1+\beta}$		$\alpha \cdot \gamma = \beta$

CONCEPT OF FEEDBACK

When some part of output signal is fed back to the input of amplifier then this process is known as feedback.

Feedback of two types :

- **Positive feedback**

When input and output are in the same phase then positive feedback is there. It is used in oscillators.

Voltage gain after feedback $A_f = \frac{A}{1 - A\beta}$

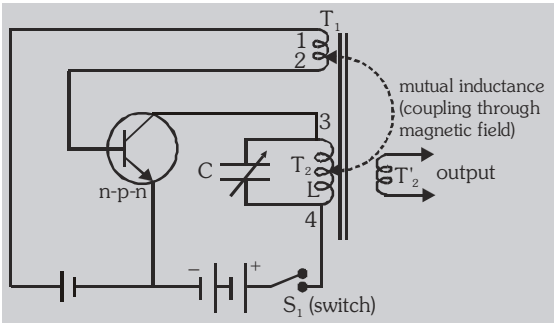
- **Negative feedback**

If input and output are out of phase and some part of that is feedback to input then it is known as negative feedback. It is used to get constant gain amplifier.

Votage gain after feedback $A_f = \frac{A}{1 + A\beta}$

3. Transistor as an Oscillator

Oscillator is device which delivers ac output wave form of desired frequency without any external input wave form.



The electric oscillations are produced by L– C circuit (i.e. tank circuit containing inductor and capacitor). These oscillations are damped one i.e. their amplitude decrease with the passage of time due to the small resistance of the inductor. In other words, the energy of the L – C oscillations decreases. If this loss of energy is compensated from outside, then undamped oscillations (of constant amplitude) can be obtained.

This can be done by using feed back arrangement and a transistor amplifier in the circuit.

Oscillating frequency of oscillator is given by $f = \frac{1}{2\pi\sqrt{LC}}$

ADVANTAGES OF SEMICONDUCTOR DEVICES OVER VACUUM TUBES

Advantages

- Semiconductor devices are very small in size as compared to the vacuum tubes. Hence the circuits using semiconductor devices are more compact.
- In vacuum tubes, current flows when the filament is heated and starts emitting electrons. So, we have to wait for some time for the operation of the circuit. On the other hand, in semiconductor devices no heating is required and the circuit begins to operate as soon as it is switched on.
- Semiconductor devices require low voltage for their operation as compared to the vacuum tube. So a lot of electrical power is saved.
- Semiconductor devices do not produce any humming noise which is large in case of vacuum tube.
- Semiconductor devices have longer life than the vacuum tube. Vacuum tube gets damaged when its filament is burnt.
- Semiconductor devices are shock proof.
- The cost of production of semiconductor-devices is very small as compared to the vacuum tubes.
- Semiconductor devices can be easily transported as compared to vacuum tube.

Disadvantages

- Semiconductor devices are heat sensitive. They get damaged due to overheating and high voltages. So they have to be housed in a controlled temperature room.
- The noise level in semiconductor devices is very high.
- Semiconductor devices have poor response in high frequency range.

INTEGRATED CIRCUIT (IC)

An integrated circuit (ICs), sometimes called a chip or microchip, is semiconductor wafer on which thousands or millions of tiny resistors, capacitors and transistors are fabricated. An IC can function as an amplifier, oscillator, timer, counter, computer memory, or microprocessor. ICs can be made very compact, having up to several billion transistors and other electronic components in an area the size of a fingernail. The most widely used technology is the Monolithic Integrated Circuit. The word monolithic is a combination of two Greek words, monos means single and lithos means stone. This, in effect means that the entire circuit is formed on a single silicon crystal (or chip). The chip dimensions are as small 1mm × 1mm or it could even be smaller.

Depending upon the level of integration (i.e., the number of circuit components or logic gates), the ICs are termed as Small integration, SSI (logic gates < 10); Medium Scale Integration, MSI (logic gates < 100); Large Scale Integration, LSI (logic gates < 1000) and very Large Scale Integration, VLSI (logic gates > 1000). The technology of fabrication is very involved but large scale industrial production has made them very inexpensive.

GOLDEN KEY POINTS

- In transistor, reverse bias is high as compared to forward bias so that the charge carriers move from emitter to base easily enter in collector region so base current is very less.
- CE configuration is widely used becasue it have large voltage and power gain as compared to other amplifiers.
- CC is used for impdence matching for connecting two transistors in cascade.

Illustrations

Illustration 14.

Explain following these questions

(i) A transistor is a current operated device. Explain why ?

(ii) In a transistor, reverse bias is quite high as compared to the forward bias. Why ?

(iii) A transistor is a temperature sensitive device. Explain.

(iv) The use of a transistor in common-emitter configuration is preferred over the common-base configuration. Explain why ?

(v) Why we prefer transistor over the vacuum tubes in the portable radio receivers ?

(vi) Why a transistor cannot be used as a rectifier ?

(vii) Why is a transistor so called ?

(viii) The base region of a transistor is lightly doped. Explain why ?

or

In a transistor, the base is lightly doped. Explain why ?

(ix) Explain why the emitter is forward biased and the collector is reverse biased in a transistor ?

Solution

(i) The action of a transistor is controlled by the charge carriers (electrons or holes). That is why a transistor is a current operated device.

(ii) In a transistor, charge carriers (electrons or holes) move from emitter to collector through the base. The reverse bias on collector is made quite high so that it may exert a large attractive force on the charge carriers to enter the collector region. These moving carriers in the collector constitute a collector current.

(iii) In a transistor, conduction is due to the movement of current carriers electrons and holes. When temperature of the transistor increases, many covalent bonds may break up, resulting in the formation of more electrons and holes. Thus, the current will increase in the transistor. This current gives rise to the production of more heat energy. the excess heat causes complete breakdown of the transistor.

(iv) The current gain and voltage gain in the common-emitter configuration is more one, So maximum power gain in common emitter configuration.

(v) This is because of two reasons :

(i) Transistor is compact and small in size than the vacuum tube.

(ii) Transistor can operate even at low voltage which can be supplied with two or three dry cells.

(vi) If transistor is to be used as a rectifier then either emitter-base or base-collector has to used as diode. For equated working of the said set of diodes, the number density of charge carriers in emitter and base or base and collector must be approximately same. As base is lightly doped and comparatively thin, so transistor cannot work as a rectifier.

(vii) The word Transistor can be treated as short form of two words 'transfer resistor'. In a transistor, a signal is introduced in the low resistance circuit and output is taken across the high resistance circuit. Thus, a transistor helps to transfer the current from low resistance part to the high resistance part.

(viii) In a transistor, the majority carriers (holes or electrons) from emtter region move towards the collector region through base. If base is made thick and highly doped, then majority of carriers from emitter will combine with the carriers in the base and only small number of carriers will reach the collector. Thus the output or collector current will be considerably small. To get large output or collector current, base is made thin and lightly doped so that only few electron-hole combination may take place in the base region.

(ix) In a transistor, the charge carriers move from emitter to collector. The emitter sends the charge carriers and collector collects them. This can happen only if emitter is forward biased and the collector is reverse biased so that it may attract the carriers.

Illustration 15.

In a transistor, the value of β is 50. Calculate the value of α.

Solution

$$\beta = \frac{\alpha}{1-\alpha} \quad \Rightarrow \quad 50 = \frac{\alpha}{1-\alpha} \quad \Rightarrow \quad 50 - 50\,\alpha = \alpha \quad \Rightarrow \quad \alpha = \frac{50}{51} = 0.98$$

Illustration 16.

Calculate the emitter current for which $I_B = 20\ \mu A$, $\beta = 100$

Solution

$I_C = \beta I_B = 100 \times 20 \times 10^{-6} = 2000\ \mu A$

$I_E = I_B + I_C = 20 + 2000 = 2020\ \mu A = 2.02 \times 10^{-3}\ A = 2.02\ mA$

Illustration 17.

The base current is 100 μA and collector current is 3 mA.

(a) Calculate the values of β, I_E and α

(b) A change of 20 μA in the base current produces a change of 0.5 mA in the collector current. Calculate $\beta_{a.c.}$.

Solution

(a) $\beta = \frac{I_C}{I_B} = \frac{3\times10^{-3}}{100\times10^{-6}} = 30,\ \alpha = \frac{\beta}{1+\beta} = \frac{30}{1+30} = \frac{30}{31} = 0.97$ and $I_E = \frac{I_C}{\alpha} = \frac{3\times31}{30} = 3.1$ mA

(b) $\Delta I_B = 20\ \mu A = 0.02$ mA , $\Delta I_C = 0.5$ mA $\therefore\ \beta_{ac} = \frac{\Delta I_C}{\Delta I_B} = \frac{0.5}{0.02} = 25$

Illustration 18.

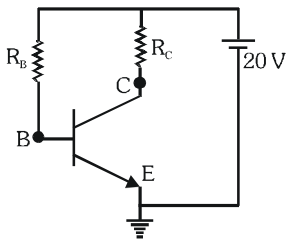
In a transistor connected in common emitter mode $R_0 = 4\ k\Omega$, $R_i = 1\ k\Omega$, $I_C = 1$ mA and $I_B = 20\ \mu A$. Find the voltage gain.

Solution

Voltage gain $A_V = \beta\left(\frac{R_0}{R_i}\right) = \left(\frac{I_C}{I_B}\right)\left(\frac{R_0}{R_i}\right) = \left(\frac{1\times10^{-3}}{20\times10^{-6}}\right)\left(\frac{4}{1}\right) = 200$

Illustration 19.

For given CE biasing circuit, if voltage across collector–emitter is 12 V and current gain is 100 and base current is 0.04 mA then determine the value of collector resistance R_C.



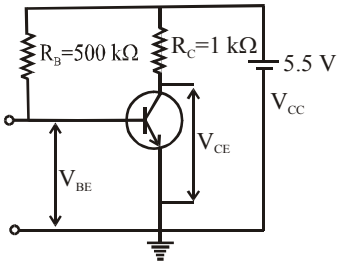
Solution

$\because\ V_{CE} = V_{CC} - I_C \times R_C$

$\therefore\ R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{V_{CC} - V_{CE}}{\beta I_B} = \frac{20-12}{100\times0.04\times10^{-3}} = 2k\Omega$

Illustration 20.

For given transistor circuit, the base current is 10 μA and the collector current is 5.2 mA. Can this transistor circuit be used as a voltage amplifier. Your answer must be supported with proper calculations. **[AIPMT (Mains) 2008]**



Solution

No, it can't be used as an amplifier

Explaination

$V_{BE} = 5.5 - I_B R_B = 5.5 - 10\times10^{-6}\times500\times10^{3} = 0.5$ V

$V_{CE} = 5.5 - I_C R_C = 5.5 - 5.2\times10^{-3}\times1\times10^{3} = 0.3$ V

It can't be used as an amplifier as both the emitter-base function and collector function are forward bias.

Illustration 21.

Two amplifiers are connected one after the other in series (cascaded). The first amplifier has a voltage gain of 10 and the second has a voltage gain of 20. If the input signal is 0·01 volt, calculate the output signal.

Solution. $\because\ A = A_1 \times A_2 = 10\times20 = 200$

$\therefore$ Output signal $= A \times$ input signal $= 200\times0{\cdot}01 = 2$ V

BEGINNER'S BOX-4

1. For a common emitter amplifier, current gain = 50. If the emitter current is 6.6 mA, calculate the collector and base current. Also calculate current gain, when emitter is working as common base amplifier.

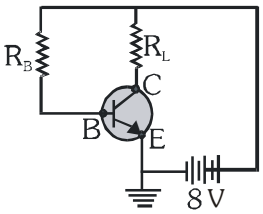
2. Transistor with $\beta = 75$ is connected to common-base configuration. What will be the maximum collector current for an emitter current of 5 mA ?

3. In npn transistor circuit, the collector current is 10 mA. If 95% of the electrons emitted reach the collector, what is the base current ?

4. In an NPN transistor 10^{10} electrons enter the emitter in 10^{-6} s and 2% electrons recombine with holes in base, then current gain α and β are :

5. For a CE amplifier, current gain is 69. If the emitter current is 7 mA then calculate the base current and collector current. **[AIPMT (Mains) 2008]**

6. An n-p-n transistor in a common emitter mode is used as a simple voltage amplifier with a collector connected to load resistance R_L and to the base through a resistance R_B. The collector-emitter voltage $V_{CE} = 4$ V, the base-emitter voltage $V_{BE} = 0.6$ V, Current through collector is 4 mA and the current amplification factor $\beta = 100$. Calculate the values of R_L and R_B.



7. A common emitter amplifier has a voltage gain of 50, an input impedance of 200 Ω and an output impedance of 400Ω. Calculate the power gain of the amplifier.

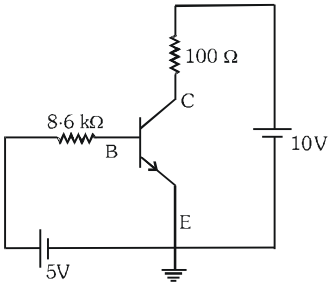
8. A silicon transistor amplifier ckt. is given here. If $\beta = 100$ then determine

(a) Base current I_B

(b) Collector current I_C

(c) V_{CE}

Take the voltage drop between base and emitter as 0.7 V.



ANSWERS

BEGINNER'S BOX-1

1. Value of R should be increased because with the increase in temperature of semiconductor as circuit resistance decreases and current tends to increase.

2. $n_e = 5 \times 10^9 m^{-3}$

3. $n_e = 5 \times 10^{22}\ m^{-3}$, $n_h = 4{\cdot}5 \times 10^9\ m^{-3}$

4. $n_e/n_h = 6/5$

BEGINNER'S BOX-2

1. (a) 0.2 eV (b) 0.1 eV (c) 0.3 eV

2. 200 Ω

3. $I_1 = 0$ and $I = I_2 = 5$mA

4. 0.25A

5. (a) $V_0 = 11.7$ V, $I = 2.34$ mA
(b) $V_0 = 11.3$ V, $I = 2.26$ mA

BEGINNER'S BOX-3

1. (1)

2. $I_S = 30$ mA, $I_L = 6$ mA, $I_Z = 24$ mA, $P_Z = 0.144$ W

3. 40 mA. **4.** 8671.33 Å

BEGINNER'S BOX-4

1. $I_C = 6.47$ mA $I_B = 0.13$ mA $\alpha = 0.98$

2. 4.93 mA **3.** 0.53 mA

4. $\alpha = 0.98$; $\beta = 49$

5. $I_B = 0.1$ mA ; $I_C = 6.9$ mA

6. 1 kΩ ;185 kΩ **7.** 1250

8. (i) 0.5 mA (ii) 50 mA (iii) 5 V

LOGIC GATES

Introduction :

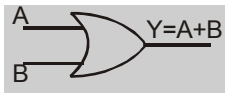
- A logic gate is a digital circuit which is based on certain logical relationship between the input and the output voltages of the circuit.
- The logic gates are built using the semiconductor diodes and transistors.
- Each logic gate is represented by its characteristic symbol.
- The operation of a logic gate is indicated in a table, known as truth table. This table contains all possible combinations of inputs and the corresponding outputs.
- A logic gate is also represented by a Boolean algebraic expression. Boolean algebra is a method of writing logical equations showing how an output depends upon the combination of inputs. Boolean algebra was invented by George Boole.

Basic Logic Gates

There are three basic logic gates. They are (1) OR gate (2) AND gate, and (3) NOT gate

- **The OR gate :-** The output of an OR gate attains the state 1 if one or more inputs attain the state 1.

Logic symbol of OR gate



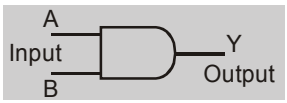
The **Boolean expression** of OR gate is Y = A + B, read as Y equals A ORing B.

Truth table of a two-input OR gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

- **The AND gate :-** The output of an AND gate attains the state 1 if and only if all the inputs are in state 1.

Logic symbol of AND gate



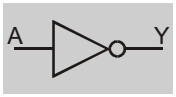
The **Boolean expression** of AND gate is Y = A.B It is read as Y equals A ANDing B

Truth table of a two-input AND gate

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

- **The NOT gate :** The output of a NOT gate attains the state 1 if and only if the input does not attain the state 1.

Logic symbol of NOT gate



The **Boolean expression** is $Y = \overline{A}$, read as Y equals NOT A.

Truth table of NOT gate

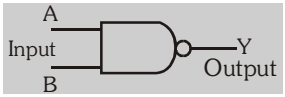
A	Y
0	1
1	0

Combination of Gates :

The three basis gates (OR, AND and NOT) when connected in various combinations give us logic gates such as NAND, NOR gates, which are the universal building blocks of digital circuits.

- **The NAND gate :**

Logic symbol of NAND gate



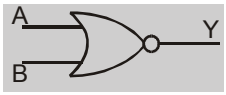
The **Boolean expression** of NAND gate is $Y = \overline{A.B}$

Truth table of a NAND gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

- **The NOR gate :**

Logic symbol of NOR gate



The **Boolean expression** of NOR gate is $Y = \overline{A + B}$

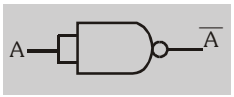
Truth table of a NOR gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Universal gates :

The NAND or NOR gate is the universal building block of all digital circuits. Repeated use of NAND gates (or NOR gates) gives other gates. Therefore, any digital system can be achieved entirely from NAND or NOR gates. We shall show how the repeated use of NAND (and NOR) gates will gives us different gates.

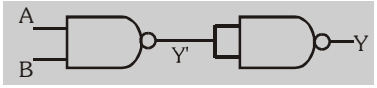
- **The NOT gate from a NAND gate :-** When all the inputs of a NAND gate are connected together, as shown in the figure, we obtain a NOT gate.



Truth table of a single input NAND gate

A	B= (A)	Y
0	0	1
1	1	0

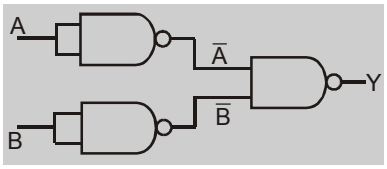
- **The AND gate from a NAND gates :-** If a NAND gate is followed by a NOT gate (i.e., a single input NAND gate), the resulting circuit is an AND gate as shown in figure and truth table given show how an AND gate has been obtained from NAND gates.



Truth table

A	B	Y'	Y
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

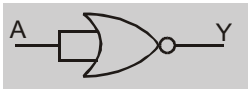
- **The OR gate from NAND gates :-** If we invert the inputs A and B and then apply them to the NAND gate, the resulting circuit is an OR gate.



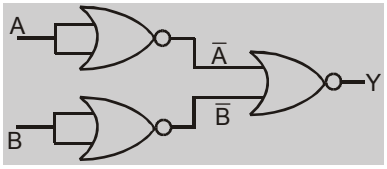
Truth table

A	B	$\bar{A}$	$\bar{B}$	Y
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

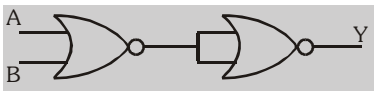
- **The NOT gate from NOR gates :-** When all the inputs of a NOR gate are connected together as shown in the figure, we obtain a NOT gate



- **The AND gate from NOR gates :-** If we invert the inputs A and B and then apply them to the NOR gate, the resulting circuit is an AND gate.



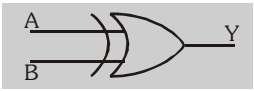
- **The OR gate from NOR gate :-** If a NOR gate is followed by a single input NOR gate (NOT gate), the resulting circuit is an OR gate.



XOR and XNOR gates :

- **The Exclusive - OR gate (XOR gate):-** The output of a two-input XOR gate attains the state 1 if one and only one input attains the state 1.

Logic symbol of XOR gate



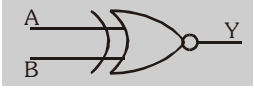
The **Boolean expression** of XOR gate is $Y = A.\bar{B} + \bar{A}.B$ or $Y = A \oplus B$

Truth table of a XOR gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

- **Exclusive - NOR gate (XNOR gate):-** The output is in state 1 when its both inputs are the same that is, both 0 or both 1.

Logic symbol of XNOR gate



The **Boolean expression** of XNOR gate is $Y = A.B + \bar{A}.\bar{B}$ or $Y = \overline{A \oplus B}$ or $A \odot B$

Truth table of a XNOR gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Laws of Boolean Algebra

Basic OR, AND, and NOT operations are given below :

OR	AND	NOT
$A + 0 = A$	$A.\ 0 = 0$	$A + \bar{A} = 1$
$A + 1 = 1$	$A.\ 1 = A$	$A\ .\ \bar{A} = 0$
$A + A = A$	$A\ .\ A = A$	$\bar{\bar{A}}\ .\ A = A$

Boolean algebra obeys commutative, associative and distributive laws as given below :

- **Commutative laws :**

  $A + B = B + A$;

  $A.B = B.A$

- **Associative laws :**

  $A + (B + C) = (A + B) + C$

  $A.\ (B\ .\ C) = (A.\ B)\ .\ C$

- **Distributive laws :**

  $A.\ (B + C) = A.B + A.C$

- **Some other useful identities :**

  (i) $A + AB = A$ (ii) $A\ .\ (A + B) = A$

  (iii) $A + (\bar{A}\ B) = A + B$ (iv) $A.\ (\bar{A} + B) = A.B$

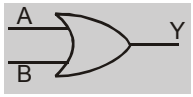
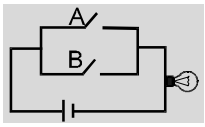
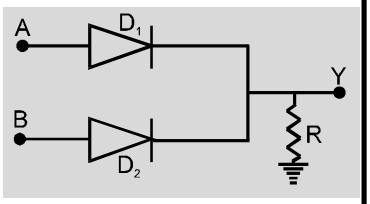
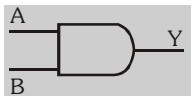
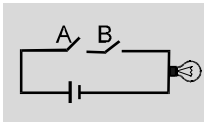
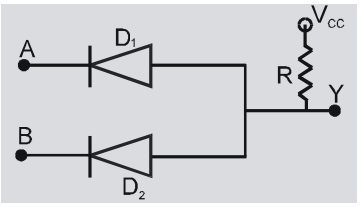
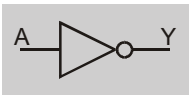
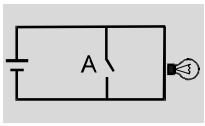
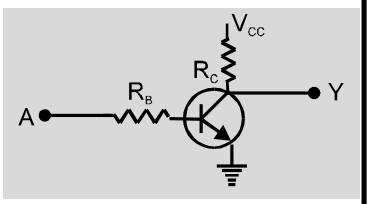
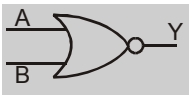
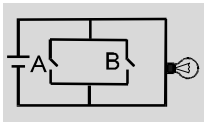
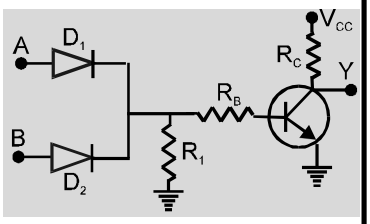
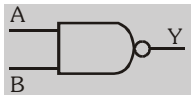
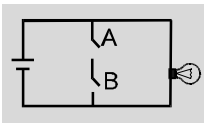
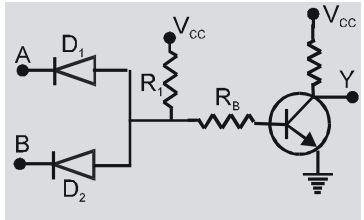
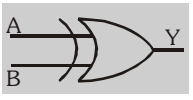
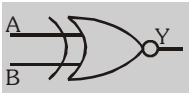
  (v) $A + (B.C) = (A + B).\ (A + C)$ (vi) $(\bar{A} + B).(A + C) = \bar{A}\ .C + B.A + B.C$

- **De Morgan's theorem :**

  First theorem : $\overline{A + B} = \bar{A}.\bar{B}$

  Second theorem : $\overline{A.B} = \bar{A} + \bar{B}$

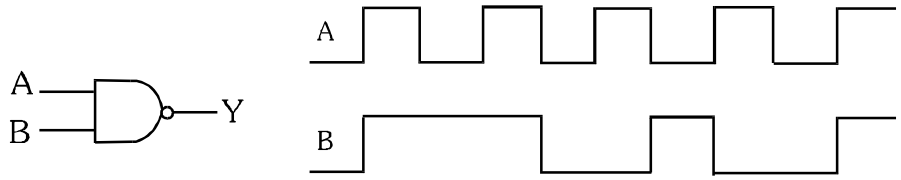
SUMMARY OF LOGIC GATES

Names	Symbol	Boolean Expression	Truth table	Electrical analogue	Circuit diagram (Practical Realisation)
OR		$Y = A + B$	A B Y 0 0 0 0 1 1 1 0 1 1 1 1		
AND		$Y = A.B$	A B Y 0 0 0 0 1 0 1 0 0 1 1 1		
NOT or Inverter		$Y = \overline{A}$	A Y 0 1 1 0		
NOR (OR +NOT)		$Y = \overline{A + B}$	A B Y 0 0 1 0 1 0 1 0 0 1 1 0		
NAND (AND+NOT)		$Y = \overline{A.B}$	A B Y 0 0 1 0 1 1 1 0 1 1 1 0		
XOR (Exclusive OR)		$Y = A \oplus B$ or $Y = \overline{A}.B + A\overline{B}$	A B Y 0 0 0 0 1 1 1 0 1 1 1 0		
XNOR (Exclusive NOR)		$Y = A \odot B$ or $Y = A.B + \overline{A}.\overline{B}$ or $Y = \overline{A \oplus B}$	A B Y 0 0 1 0 1 0 1 0 0 1 1 1		

Illustrations

Illustration 1

In the figures below, Circuit symbol of a logic gate and two input waveforms 'A' and 'B' are shown.



(a) Name the logic gate & Write its boolean expression

(b) Write its truth table

(c) Give the output wave form

Solution

(a) NAND gate ; $Y = \overline{A \cdot B}$

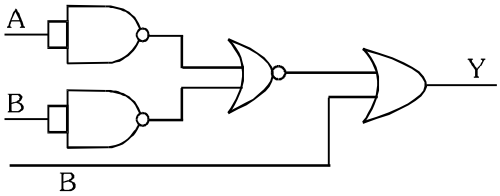
(b) Truth table

Input A	Input B	Output Y
0	0	1
0	1	1
1	0	1
1	1	0

(c) Output waveform

Illustration 2

Write down output Y in terms of inputs A and B.



Solution

$Y = \overline{\overline{A} + \overline{B}} + B = \overline{\overline{A.B}} + B = A.B + B = (A+1)\,B = B$

Illustration 3

By using Bolean Algebra prove that $\overline{A}B + A\overline{B} + AB = A + B$

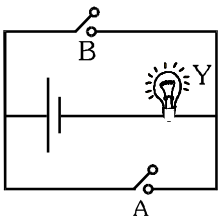
Solution

$LHS = \overline{A}B + A\overline{B} + AB = \overline{A}B + A\overline{B} + AB + AB$

$= A(B + \overline{B}) + B(\overline{A} + A) = A.1 + B.1 = A + B = RHS$

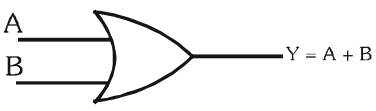
Illustration 4

Given electrical circuit is equivalent to which logic gate, also draw its symbol and truth table.



Solution

OR gate



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Illustration 5

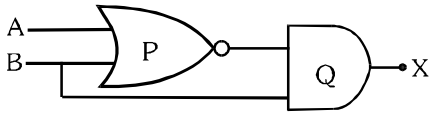
Write the truth table for the logical function D = (A AND B) OR B

Solution

A	B	X = A AND B	D = X OR B
0	0	0	0
0	1	0	1
1	0	0	0
1	1	1	1

Illustration 6

Identify the logic gates P and Q in given circuit. Also write down relation in A, B and X.

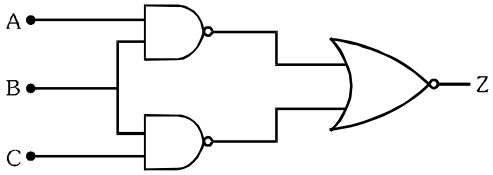


Solution

P is NOR gate & Q is AND gate, $X = \left(\overline{A+B}\right).B = (\overline{A}.\overline{B}).B = \overline{A}.(\overline{B}.B) = \overline{A}.0 = 0$

Illustration 7

Write down the equivalent function performed by given circuit. Explain your answer.



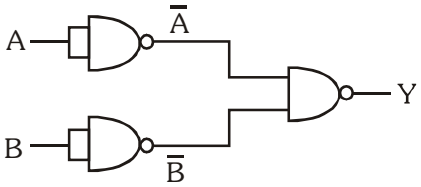
Solution

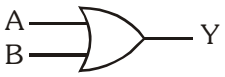
AND gate, $Z = \overline{\overline{A\cdot B}+\overline{B\cdot C}} = \overline{\overline{AB}\cdot\overline{BC}} = \overline{\overline{ABC}} = ABC \quad (\because \overline{X}+\overline{Y} = \overline{X\cdot Y})$

Illustration 8

If inputs A and B are inverted before entering into NAND gate as shown in diagram.

Write down the logical symbol and truth table by using A, B, $\overline{A}$, $\overline{B}$, Y. **[AIPMT 2005, 2007]**



Solution $Y = \overline{\overline{A}.\overline{B}} = A+B$ so logical symbol 

Truth table

A	B	$\overline{A}$	$\overline{B}$	Y
0	0	1	1	0
1	0	0	1	1
0	1	1	0	1
1	1	0	0	1

EXERCISE-I (Conceptual Questions)

SEMICONDUCTORS

1. On increasing the temperature the specific resistance of a semiconductor :–

(1) increases

(2) decreases

(3) does not change

(4) first decreases and then increases

2. Platinum and silicon are cooled after heating up to 25° C then :–

(1) resistance of platinum will increase and that of silicon decreases.

(2) resistance of silicon will increase and that of platinum decreases.

(3) resistance of both will decrease.

(4) resistance of both increases.

3. Electric conduction in a semiconductor takes place due to :–

(1) electrons only

(2) holes only

(3) both electrons and holes

(4) neither electrons nor holes

4. The atomic bonding is same for which of the following pairs :–

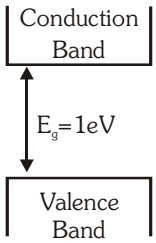
(1) Ag and Si

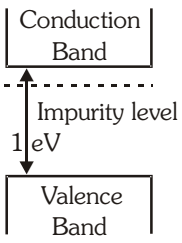
(2) Ge and Si

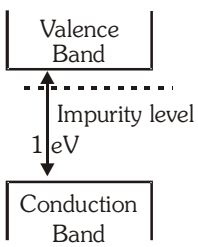
(2) Ne and Ge

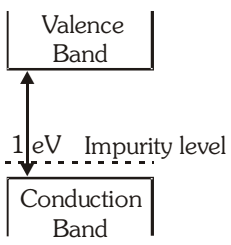
(4) NaCl and Ge

5. Which of the following energy band diagram shows the n-type semiconductor :–

(1)


(2)


(3)


(4)


6. Let n_p and n_e be the numbers of holes and conduction electrons in an extrinsic semiconductor.

(1) $n_p > n_e$ (2) $n_p = n_e$

(3) $n_p < n_e$ (4) $n_p \neq n_e$

7. A p-type semiconductor is :–

(1) positively charged

(2) negatively charged

(3) uncharged

(4) uncharged at 0K but charged at higher temperatures

8. Which statement is correct for p -type semiconductor

(1) the number of electrons in conduction band is more than the number of holes in valence band at room temperature

(2) the number of holes in valence band is more than the number of electrons in conduction band at room temperature

(3) there are no holes and electrons at room temperature

(4) number of holes and electrons is equal in valence and conduction band

9. When an impurity is doped into an intrinsic semiconductor, the conductivity of the semiconductor :

(1) increases (2) decreases

(3) remains the same (4) become zero

10. When we convert pure semiconductor into N type the number of hole :–

(1) Increases (2) Decreases

(3) Remains constant (4) None

11. A semiconductor is damaged by a strong current, because :–

(1) lack of free electrons (2) decrease in electrons

(3) excess of electrons (4) none of these

12. If n_e and n_h are the number of electrons and holes in a semiconductor heavily doped with phosphorus, then :–

(1) $n_e >> n_h$ (2) $n_e << n_h$

(3) $n_e \leq n_h$ (4) $n_e = n_h$

13. Two wires P and Q made up of different materials have same resistance at room temperature. When heated, resistance of P increases and that of Q decreases. We conclude that:–

(1) P and Q both are conductors but because of being made of different materials it happens so.

(2) P is n-type semiconductor and Q is p-type semiconductor.

(3) P is semiconductor and Q is conductor.

(4) P is conductor and Q is semicondcutor.

14. When the conductivity of a semiconductor is only due to breaking of covalent bonds, the semiconductor is called :–

(1) intrinsic (2) extrinsic

(3) p-type (4) n-types

15. In an intrinsic semiconductor, number of electrons and holes at room temperature are :–

(1) equal (2) zero

(3) unequal (4) infinity

16. A semiconductor wire is connected in an electric circuit in series and temperature of semiconductor increased then the current in the circuit :–

(1) decreases (2) constant

(3) increases (4) will not flow

17. In germanium crystal, the forbidden energy gap in joule is :–

(1) 1.6×10^{-19} (2) zero

(3) 1.12×10^{-19} (4) 1.76×10^{-19}

18. In semiconductor, at room temperature :–

(1) valence band are partially empty and conduction band are partially filled

(2) valence band are fully filled and conduction band are partially empty

(3) valence band are fully filled

(4) conduction band are fully empty

19. The probability of electrons to be found in the conduction band of an intrinsic semiconductor at a finite temperature :–

(1) decreases exponentially with increasing band gap.

(2) increases exponentially with increasing band gap.

(3) decrease with increasing temperature.

(4) is independent of the temperature and the band gap.

20. In a p-type semicondutor, there are mainly :–

(1) free electrons (2) holes

(3) both (1) and (2) (4) none of these

21. A conducting wire of Copper and Germanium are cooled from room temperature to temperature 80K, then their resistance will :–

(1) increase

(2) decrease

(3) copper's increase and Germanium's decrease

(4) copper's decrease and Germanium's increase

22. Choose the false statement from the following :-

(1) the resistivity of a semiconductor increases with increase in temperature.

(2) substances with energy gap of the order of 10 eV are insulators.

(3) in conductors the valence and conduction bands may over lap.

(4) the conductivity of a semiconductor increases with increases in temperature.

23. Carbon, Silicon and Germanium atoms have four valence electrons each. Their valence and conduction bonds are separated by energy band gaps represented by $(E_g)_C$, $(E_g)_{Si}$ and $(E_g)_{Ge}$ respectively. Which one of the following relationships is true in their case :–

(1) $(E_g)_C < (E_g)_{Ge}$ (2) $(E_g)_C > (E_g)_{Si}$

(3) $(E_g)_C = (E_g)_{Si}$ (4) $(E_g)_C < (E_g)_{Si}$

24. In semiconducting material the mobilities of electrons and holes are μ_e and μ_h respectively. Which of the following is true :–

(1) $\mu_e > \mu_h$ (2) $\mu_e < \mu_h$

(3) $\mu_e = \mu_h$ (4) $\mu_e < 0; \mu_h > 0$

25. Impurity energy level of n-type semiconductor lies in:-

(1) just above valence band

(2) just below conduction band

(3) between valence and conduction band

(4) none of these

26. What is the energy gap in Si semiconductor?

(1) 4.4 eV (2) 0.3 eV

(3) 0.7 eV (4) 1.1 eV

PN JUNCTION & BIASING OF DIODE

27. Region which have no free electrons and holes in a p-n junction is :–

(1) p - region (2) n - region

(3) junction (4) depletion region

28. In p-n junction at the near at junction there are :-

(1) positive Ions

(2) negative Ions

(3) positive and negative Ions

(4) electrons and holes

29. Depletion layer in p-n junction region is caused by

(1) drift holes

(2) diffusion of free carriers

(3) migration of impurity ions

(4) drift of electrons

30. In a P–N Junction diode not connected to any circuit

(1) potential is the same every where.

(2) the P - type side is at a higher potential than the N - type side.

(3) there is an electric field at the junction directed from the N - type side to the P - type side.

(4) there is an electric field at the junction directed from the P - type side to the N - type side.

31. The minority current in a p-n junction is :–

(1) from the n-side to the p-side

(2) from the p-side to the n-side

(3) from the n-side to the p-side if the junction is forward-biased and in the opposite direction if it is reverse biased.

(4) from the p-side to the n-side if the junction is forward-biased and in the opposite direction if it is reverse biased

32. The majority current in a p-n junction is :–

(1) from the n-side to the p-side

(2) from the p-side to the n-side

(3) from the n-side to the p-side if the junction is forward-biased and in the opposite direction if it is reverse biased

(4) from the p-side to the n-side if the junction is forward-biased and in the opposite direction if it is reverse biased

33. Diffusion current in a p-n junction is greater than the drift current in magnitude :–

(1) if the junction is forward-biased

(2) if the junction is reverse-biased

(3) if the junction is unbiased

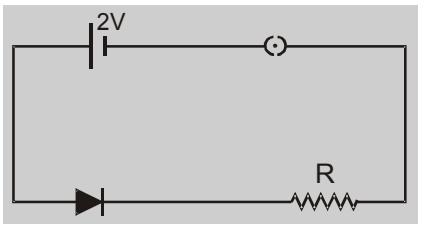
(4) in no case

34. In a ..... biased P-N junction, the net flow holes is from N-region to the P-region :–

(1) F.B. (2) R. B.

(3) Unbiased (4) both 1 & 2

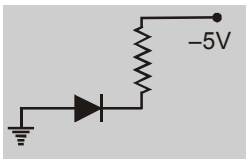
35. A 2 V battery forward biases a diode however there is a drop of 0.5 V across the diode which is independent of current. Also a current greater then 10 mA produces large joule loss and damages diode. If diode is to be operated at 5 mA, the series resistance to be put is :–

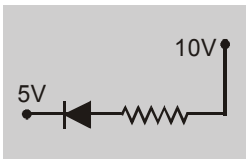


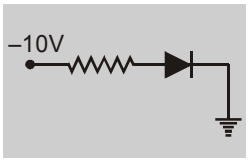
(1) 3 kΩ (2) 300 kΩ

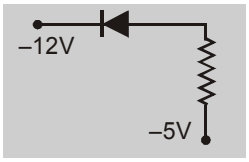
(3) 300 Ω (4) 200 kΩ

36. Which of the following diode is reverse biased :–

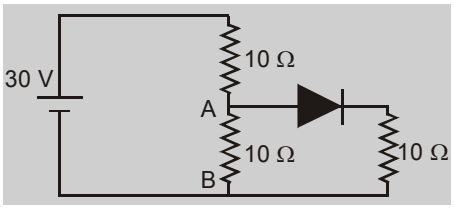
(1) 

(2) 

(3) 

(4) 

37. Find V_{AB} :–



(1) 10 V (2) 20 V (3) 30 V (4) none

38 Assuming that the junction diode is ideal then the current through the diode is:-

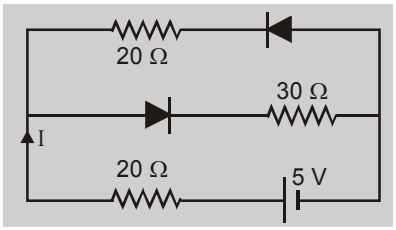
(1) 200 mA (2) 20 mA (3) 2 mA (4) zero

39. The resistance of a reverse biased pn junction diode is about :–

(1) 1 ohm (2) 10^2 ohm

(3) 10^3 ohm (4) 10^6 ohm

40. Current I in the circuit will be :–



(1) $\frac{5}{40}$ A (2) $\frac{5}{50}$ A (3) $\frac{5}{10}$ A (4) $\frac{5}{20}$ A

41. In a p-n junction the depletion layer of thickness 10^{-6} m has potential across it is 0.1 V. The average electric field is (V/m) :–

(1) 10^7 (2) 10^{-6} (3) 10^5 (4) 10^{-5}

42. In a unbias p-n junction :-

(1) high potential is at n side and low potential is at p side.

(2) high potential is at p side and low potential is at n side.

(3) p and n both are at same potential.

(4) undetermined.

43. On increasing the reverse bias to a large value in p-n junction diode then value of current

(1) remains fixed (2) increases slowly

(3) decrease slowly (4) suddenly increase

44. Reverse bias applied to a junction diode :–

(1) lowers the potential barrier.

(2) raises the potential barrier.

(3) increases the majority carrier current.

(4) increases the minority carrier current.

45. Correct statement for diode is :–

(1) in full wave rectifier both diodes work alternatively.

(2) in full wave rectifier both diodes work simultaneously.

(3) efficiency of full wave rectifier and half wave rectifier is same.

(4) full wave rectifier in bidirectional.

46. When a junction diode is reverse biased, the flow of current across the junction is mainly due to :–

(1) diffusion of charges

(2) depends upon the nature of material

(3) drift of charges

(4) both drift and diffusion of charges

47. The width of depletion region in a p-n junction diode

(1) increases when reverse bias is applied.

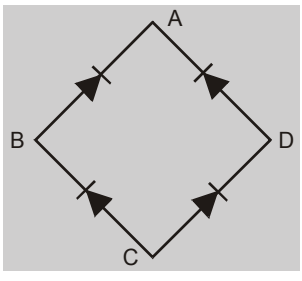
(2) increases when a forward bias is applied.

(3) decreases when a reverse bias is applied.

(4) remains the same irrespective of the bias voltage.

SPECIAL TYPES OF DIODES

48. For the given circuit shown in fig, to act as full wave rectifier :– a.c. input should be connected across ..... and ..... the d.c. output would appear across ..... and .....



(1) A, C, B, D (2) B, D, A, C

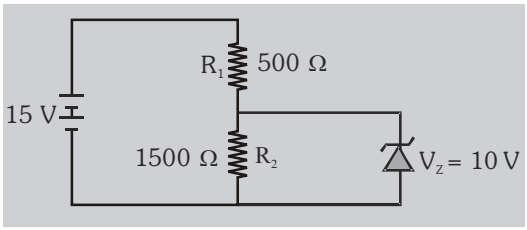
(3) A, B, C, D (4) C, A, D, B

49. Forbidden energy gap of Ge is 0.75 eV, maximum wave length of incident radiation of photon for producing electron - hole pair in germanium semiconductor is :–

(1) 4200 Å (2) 16500 Å

(3) 4700 Å (4) 4000 Å

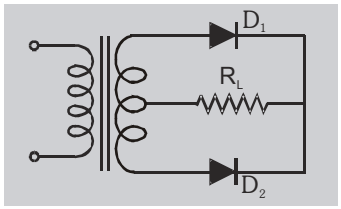
50. In the circuit given the current through the zener diode is :-

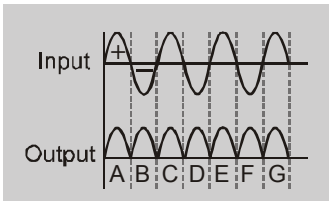


(1) 10 mA (2) 6.67 mA

(3) 5 mA (4) 3.33 mA

51. A full wave rectifier circuit along with the input and output voltage is shown in the figure then output due to diode D_2 is :–





(1) A, C (2) B, D (3) B, C (4) A, D

52. If a full wave rectifier circuit is operating from 50 Hz mains, the fundamental frequency in the ripple will be :–

(1) 25 Hz (2) 50 Hz

(3) 70.7 Hz (4) 100 Hz

53. The electrical circuit used to get smooth DC output from a rectifier circuit is called :–

(1) filter (2) oscillator

(3) logic gate (4) amplifier

54. When two semiconductor of p and n type are brought into contact, they form a p-n junction which acts like a :–

(1) rectifier (2) amplifier

(3) oscillator (4) conductor

55. In p-n junction photocell electromotive force due to monochromatic light is proportional to

(1) p-n potential barrier

(2) intensity of light

(3) frequency of light

(4) p-n applied voltage

56. Efficiency of a half wave rectifier is nearly :–

(1) 80 % (2) 60 % (3) 40 % (4) 20 %

57. Zener dode is used for :–

(1) rectification

(2) stabilization

(3) amplification

(4) producing oscillations in an oscillator

TRANSISTOR

58. A transistor is used in the common emitter mode as an amplifier then :–

(A) the base emitter junction is forward baised.

(B) the base emitter junction is reverse baised.

(C) the input signal is connected in series with the voltage applied to bias the base emitter junction.

(D) the input signal is connected in series with the voltage applied to bias the base collector junction.

(1) A, B (2) A, D

(3) A, C (4) only C

59. In a transistor :–

(1) the emitter has the least concentration of impurity.

(2) the collector has the least concentration of impurity.

(3) the base has the least concentration of impurity.

(4) all the three regions have equal concentration of impurity.

60. In transistor symbols, the arrows shows the direction of :-

(1) current in the emitter

(2) electron current in the emitter

(3) holes current in the emitter

(4) electron current in the emitter

61. The region of transistor in which extra impurity is doped to obtain a large number of majority carrier is called as :–

(1) emitter

(2) base

(3) collector

(4) any one of these depending upon the transistor

62. An oscillator is nothing but an amplifier with :–

(1) positive feedback (2) high gain

(3) no feedback (4) negative feedback

63. Input resistance of common emitter transistor compare with output resistance is :–

(1) less (2) more

(3) less and more (4) none of these

64. The current gain β of a transistor is 50. The input resistance of the transistor, when used in the common emitter configuration, is 1 kΩ. The peak value of the collector a.c. current for an alternating peak input voltage 0.01 V is :–

(1) 100 μA (2) 250 μA

(3) 500 μA (4) 800 μA

65. A transistor is operated in CE configuration at V_{CC}=2 V such that a change in base current from 100 μA to 200 μA produces a change in the collector current from 9 mA to 16.5 mA. The value of current gain, β is :–

(1) 45 (2) 50 (3) 60 (4) 75

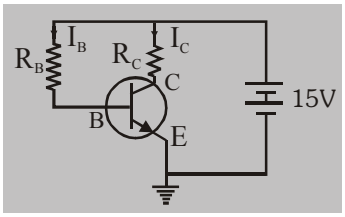
66. The input resistance of a silicon transistor is 1 kΩ. If base current is changed by 100 μA, it causes the change in collector current by 2 mA. This transistor is used as a CE amplifier with a load resistance of 5 kΩ. What is the ac voltage gain of amplifier ?

(1) 10 (2) 100 (3) 500 (4) 200

67. For a transistor amplifier power gain and voltage gain are 7.5 and 2.5 respectively. The value of the current gain will be :–

(1) 0.33 (2) 0.66 (3) 0.99 (4) 3

68. In the following common emitter circuit if β = 100, V_{CE} = 7 V, V_{BE} = negligible, R_C = 2 kΩ then I_B is :-



(1) 0.01 mA (2) 0.04 mA

(3) 0.02 mA (4) 0.03 mA

69. When a transistor is used in a circuit :

(1) both junctions are forward biased.

(2) emitter base junction is forward biased and the base collector junction is reverse biased.

(3) emitter base junction is reverse biased and the base collector junction is forward biased.

(4) both junctions are reverse biased.

70. What is the voltage gain in a common emitter amplifier where input resistance is 3 Ω and load resistance is 24 Ω and current gain β = 6 ?

(1) 2.2 (2) 1.2

(3) 4.8 (4) 48

71. In a n-p-n transistor circuit, the collector current is 10 mA. If 90% of the electrons emitted reach the collector then the emitter current (I_E) and base current (I_B) are given by :–

(1) I_E = 1 mA; I_B = 11 mA

(2) I_E = 11 mA ; I_B = 1 mA

(3) I_E = –1 mA; I_B = 9 mA

(4) I_E = 9 mA ; I_B = –1 mA

72. In a transistor, the base is made very thin and lightly doped with an impurity :–

(1) to save the transistor from heating effect

(2) to enable the emitter to emit small number of electrons and holes

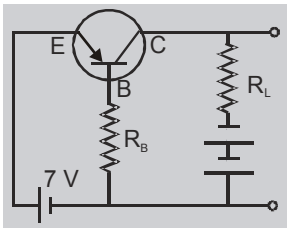
(3) to enable the collector to collect 95% of the holes or electron coming from the emitter side

(4) none of the above

73. In CB configuration of transistor ac current gain is $\frac{\Delta i_C}{\Delta i_E}$=0.98, determine current gain of CE configuration :–

(1) 49 (2) 98 (3) 4.9 (4) 24.5

74. In the given transistor circuit, the base current is 35 μA. The value of R_B is (V_{BE} is assumed to negligible)



(1) 100 kΩ (2) 300 kΩ

(3) 200 kΩ (4) 400 kΩ

75. In an n-p-n transistor :–

(1) holes move from emitter to base

(2) electrons moves from emitter to base

(3) holes move from base to collector

(4) electrons move from collector to base

76. In the study of transistor as amplifier if $\alpha = \frac{I_C}{I_E}$ and $\beta = \frac{I_C}{I_B}$ where I_C, I_B, and I_E are the collector, base and emitter current, then :–

(1) $\beta = \frac{\alpha}{1+\alpha}$ (2) $\beta = \frac{\alpha}{1-\alpha}$

(3) $\beta = \frac{1+\alpha}{\alpha}$ (4) $\beta = \frac{1-\alpha}{\alpha}$

77. In the CB mode of a transistor, when the collector voltage is changed by 0.5 volt, the collector current changes by 0.05 mA. the output resistance will be

(1) 10 kΩ (2) 20 kΩ (3) 5 kΩ (4) 2.5 kΩ

78. A n-p-n transistor conducts when :–

(1) both collector and emitter are positive with respect to the base.

(2) collector is positive and emitter is negative with respect to the base.

(3) collector is positive and emitter is at same potential as the base.

(4) both collector and emitter are negative with respect to the base.

79. In the case of constants α and β of a transistor :–

(1) $\alpha = \beta$ (2) $\beta < 1$ $\alpha > 1$

(3) $\alpha\beta = 1$ (4) $\beta > 1$ $\alpha < 1$

80. For a transistor in a common emitter arrangement the alternating current gain β is given by :–

(1) $\beta = \left[\frac{\Delta I_C}{\Delta I_E}\right]_{V_{CE}}$ (2) $\beta = \left[\frac{\Delta I_B}{\Delta I_C}\right]_{V_{CE}}$

(3) $\beta = \left[\frac{\Delta I_C}{\Delta I_B}\right]_{V_{CE}}$ (4) $\beta = \left[\frac{\Delta I_E}{\Delta I_C}\right]_{V_{CE}}$

81. Consider an n–p–n transistor amplifier in common–emitter configuration. The current gain of the transistor is 100. If the collector current changes by 1 mA, what will be the change in emitter current ?

(1) 1·1 mA (2) 1·01 mA

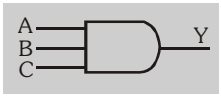
(3) 0·01 mA (4) 10 mA

LOGIC GATE

82. The output of the given logic gate is 1 when inputs A, B and C are such that :–

(1) A = 1, B = 0, C = 1

(2) A = 1, B = 1, C = 0



(3) A = B = C = 0

(4) A = B = C = 1

83. A two inputed XOR gate produces an high output only when its both inputs are :–

(1) same (2) different

(3) low (4) high

84. Which of the following Boolean expression is not correct :–

(1) $\overline{\bar{A}.\bar{B}} = A + B$ (2) $\overline{\overline{A+B}} = A \cdot B$

(3) $\overline{\overline{A.B}} = A.B$ (4) $\bar{1} + \bar{1} = 1$

85. In Boolean algebra, which of the following is not equal to zero :–

(1) $A.\bar{A}$ (2) A.0 (3) $\overline{A+\bar{A}}$ (4) $\overline{\bar{A}.0}$

86. Digital circuits can be made by repetative use of :–

(1) OR gate (2) AND gate

(3) NOT gate (4) NAND gate

87. The truth table shown below is for which of the following gates :–

A	B	Y
1	1	1
0	1	0
1	0	0
0	0	1

(1) XNOR

(2) AND

(3) XOR

(4) NOR

88. When all the inputs of a NAND gate are connected together, the resulting circuit is :–

(1) a NOT gate (2) an AND gate

(3) an OR gate (4) a NOR gate

89. A NAND gate followed by a NOT gate is :–

(1) an OR gate (2) an AND gate

(3) a NOR gate (4) a XOR gate

90. The NOR gate is logically equivalent to an OR gate followed by :–

(1) an inverter (2) a NOR gate

(3) a NAND gate (4) All of above

91. The output of a two input NOR gate is in state 1 when :–

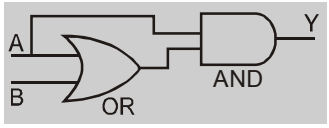
(1) either input terminals is at 0 state

(2) either input terminals is at 1 state

(3) both input terminals are at 0 state

(4) both input terminals are at 1 state

92. The output Y of the combination of gates shown is equal to :–



(1) A

(2) $\bar{A}$

(3) A + B

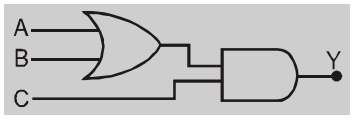
(4) AB

93. What would be the output of the circuit whose Boolean expression $Y = A\bar{B} + AB$ when A = 1, B = 0 :–

(1) 1 (2) 0

(3) both (1) & (2) (4) none of these

94. To get an output 1, the input ABC should be :–

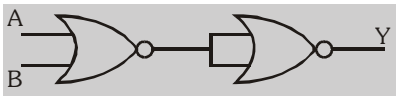


(1) 101 (2) 100 (3) 110 (4) 010

95. The output of 2 input gate is 1 only if its inputs are equal. It is true for :–

(1) NAND (2) AND (3) EX-NOR (4) EX-OR

96. The circuit shown here is logically equivalent to :–



(1) OR gate (2) AND gate

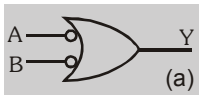
(3) NOT gate (4) NAND gate

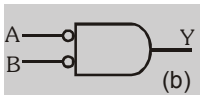
97. A two-input NAND gate is followed by a single-input NOR gate. This logic circuit will function as :–

(1) an AND gate (2) an OR gate

(3) a NOT gate (4) a NOR gate

98. The logic symbols shown here are logically equivalent to :–





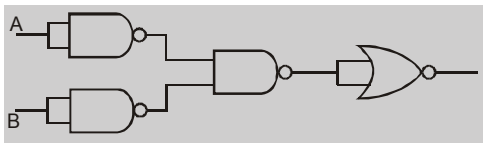
(1) (a) AND and (b) OR gate

(2) (a) NOR and (b) NAND gate

(3) (a) OR and (b) AND gate

(4) (a) NAND and (b) NOR gate

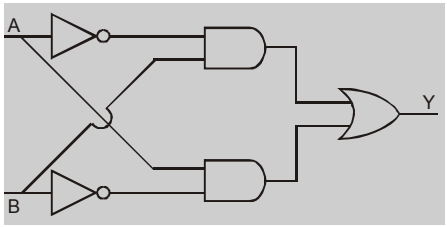
99. The combination of the gates shown will produce



(1) OR gate (2) AND gate

(3) NOR gate (4) NAND gate

100. The combination of the gates shown will produce



(1) AND gate (2) NAND gate

(3) NOR gate (4) XOR gate

101. The truth table for the following combination of gates is :-

(1)

A	B	Y
0	0	0
0	1	0
1	0	1
1	1	1

(2)

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

(3)

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(4)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

102. In the Boolean algebra $\bar{A}.\bar{B}$ equals :–

(1) A + B (2) $\overline{A+B}$

(3) A . B (4) $\bar{A}.B$

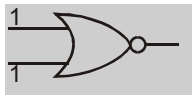
103. How many NOR gates are required to form NAND gate :–

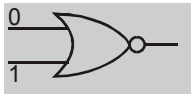
(1) 1 (2) 3 (3) 2 (4) 4

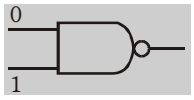
104. How many NAND gates are used to form AND gate :–

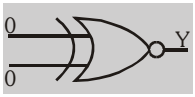
(1) 3 (2) 2 (3) 1 (4) 4

105. Which of the following gates will have an output of 1 :–

(a) 

(b) 

(c) 

(d) 

(1) (a) and (b) (2) (b) and (c)

(3) (c) and (d) (4) (a) and (d)

106. The logic behind 'NOR' gate is that it gives :–

(1) high output when both inputs are high

(2) high output when both inputs are low

(3) low output when both inputs are low

(4) none of these

107. Logic gates are the building blocks of a :–

(1) abacus system (2) analog system

(3) digital system (4) none of these

108. Boolean algebra is essentially based on :–

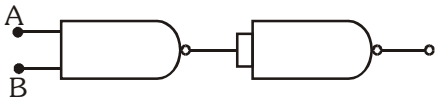
(1) logic (2) truth

(3) numbers (4) symbol

109. Out of the following, universal gate is :–

(1) NOT (2) OR (3) AND (4) NAND

110. Identify the logic operation of the following logic circuit



(1) NAND (2) AND (3) NOR (4) OR

EXERCISE-I (Conceptual Questions) ANSWER KEY

Que.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Ans.	**2**	**2**	**3**	**2**	**2**	**4**	**3**	**2**	**1**	**2**	**3**	**1**	**4**	**1**	**1**
Que.	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Ans.	**3**	**3**	**1**	**1**	**2**	**4**	**1**	**2**	**1**	**2**	**4**	**4**	**3**	**2**	**3**
Que.	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45
Ans.	**1**	**2**	**1**	**2**	**3**	**3**	**1**	**2**	**4**	**2**	**3**	**1**	**4**	**2**	**1**
Que.	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60
Ans.	**3**	**1**	**2**	**2**	**4**	**2**	**4**	**1**	**1**	**2**	**3**	**2**	**3**	**3**	**1**
Que.	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75
Ans.	**1**	**1**	**1**	**3**	**4**	**2**	**4**	**2**	**2**	**4**	**2**	**3**	**1**	**3**	**2**
Que.	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90
Ans.	**2**	**1**	**2**	**4**	**3**	**2**	**4**	**2**	**4**	**4**	**4**	**1**	**1**	**2**	**4**
Que.	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105
Ans.	**3**	**1**	**1**	**1**	**3**	**1**	**1**	**4**	**3**	**4**	**1**	**2**	**4**	**2**	**3**
Que.	106	107	108	109	110										
Ans.	**2**	**3**	**1**	**4**	**2**										

EXERCISE-II (Assertion & Reason)

Directions for Assertion & Reason questions

These questions consist of two statements each, printed as Assertion and Reason. While answering these Questions you are required to choose any one of the following four responses.

(A) If both Assertion & Reason are True & the Reason is a correct explanation of the Assertion.

(B) If both Assertion & Reason are True but Reason is not a correct explanation of the Assertion.

(C) If Assertion is True but the Reason is False.

(D) If both Assertion & Reason are false.

1. **Assertion :** Generally semiconductors do not obey Ohm's law.

Reason : Electric current is determined by the rate of flow of charge carriers.

(1) A (2) B (3) C (4) D

2. **Assertion :** Germanium is preferred over silicon for making semiconductor devices.

Reason : Energy gap for Ge is more than that of Si.

(1) A (2) B (3) C (4) D

3. **Assertion :** The temperature coefficient of resistance is positive for metals and negative for semiconductors.

Reason : On raising the temperature, in metals drift velocity decreases but in semiconductors more charge carriers are released.

(1) A (2) B (3) C (4) D

4. **Assertion :** If the temperature of a semiconductor is increased, its resistance decreases.

Reason : The energy gap between conduction band and valence band in case of semiconductor is small.

(1) A (2) B (3) C (4) D

5. **Assertion :** Conductivity of a semiconductor increases on doping.

Reason : Doping raises the temperature of semiconductor.

(1) A (2) B (3) C (4) D

6. **Assertion :** For a given applied voltage, conduction current in n-type semiconductor is more than that in p-type semiconductor.

Reason : Mobility of electrons is greater than that of holes.

(1) A (2) B (3) C (4) D

7. **Assertion :** In an unbiased p-n junction, holes diffuse from the p-region to n-region.

Reason : Hole concentration in p-region is more as compared to n-region.

(1) A (2) B (3) C (4) D

8. **Assertion :** We cannot measure the potential barrier of p-n junction by putting a sensitive voltmeter across its terminals.

Reason : In the depletion layer, there are no free electrons or holes and in the absence of forward bias, it offers infinite resistance.

(1) A (2) B (3) C (4) D

9. **Assertion :** For forward biasing, positive terminal of external battery is connected to p-type and negative terminal of external battery is connected to n-type semiconductor.

Reason : This would support the tendency of majority charge carriers to cross the junction.

(1) A (2) B (3) C (4) D

10. **Assertion :** In reverse bias, strong electric field exists across the potential barrier.

Reason : In Zener diode depletion layer is thin.

(1) A (2) B (3) C (4) D

11. **Assertion :** Two p-n junction diodes placed back to back, will work as an n-p-n transistor.

Reason : The p-region of two p-n junction diodes back to back will form the base of n-p-n transistor.

(1) A (2) B (3) C (4) D

12. **Assertion :** To be used as amplifier, the transistor in the common emitter configuration is preferred to the common base configuration.

Reason : In the common emitter, the signal is applied between emitter and base.

(1) A (2) B (3) C (4) D

13. **Assertion :** In solar cell it is imperative (essential) that photogeneration of electrons and holes occurs in depletion region.
Reason : The junction Field separates electron hole pair effectively.
(1) A (2) B (3) C (4) D

14. **Assertion :** In transistor, common emitter configuration is used to make a NOT gate.
Reason : In common emitter configuration, output voltage and input voltage have 180° phase difference.
(1) A (2) B (3) C (4) D

15. **Assertion :–** A transistor amplifier in common emitter configuration has a low input impedance.
Reason :– The base to emitter region is forward biased. **[AIIMS-2004]**
(1) A (2) B (3) C (4) D

16. **Assertion** : In a common emitter transistor amplifier the input current is much less than the output current. **[AIIMS-2005]**
Reason : The common emitter transistor amplifier has very high input impedance.
(1) A (2) B (3) C (4) D

17. **Assertion:–** In common base configuration, the current gain of the transistor is less than unity.
Reason:– The collector terminal is reverse biased for amplification. **[AIIMS-2006]**
(1) A (2) B (3) C (4) D

18. **Assertion:–** A p-n junction with reverse bias can be used as a photo-diode to measure light intensity.
Reason:– In a reverse bias condition the current is small and it is more sensitive to changes in incident light intensity. **[AIIMS-2006]**
(1) A (2) B (3) C (4) D

19. **Assertion :-** In zener diode depletion layer is thin.
Reason :- In reverse bias, strong electric field exist across the potential barrier. **[AIIMS-2010]**
(1) A (2) B (3) C (4) D

20. **Assertion :-** A transistor amplifier operates in active region. **[AIIMS-2010]**
Reason: In active region transistor characteristic is linear.
(1) A (2) B (3) C (4) D

21. **Assertion :-** Photodiode & photovoltaic cell are based on the same principle. **[AIIMS-2011]**
Reason :- Both use same method of operations to work.
(1) A (2) B (3) C (4) D

22. **Assertion :-** Transistor can be used as a switch.
Reason :- Both linear & non-linear voltage bias dependance occurs in it. **[AIIMS-2011]**
(1) A (2) B (3) C (4) D

23. **Assertion :-** In an extrinsic semiconductor dopped with pentavalent impurity and an intrinsic semiconductor number of holes are same.
Reason :- Number of holes doesn't depend on doping concentrations. **[AIIMS-2014]**
(1) A (2) B (3) C (4) D

24. **Assertion :-** Metals are better conductor than semiconductors. **[AIIMS-2015]**
Reason :- Valence band and conduction band have large energy gap in case of metals.
(1) A (2) B (3) C (4) D

25. ***Assertion :-*** Depletion Region of Zener diode is small. **[AIIMS-2016]**
Reason :- P–N junction are highly dopped. In zener diode.
(1) A (2) B (3) C (4) D

26. ***Assertion :-*** Absorption factor for GaAs is larger as compared to Si for sunlight. **[AIIMS-2017]**
Reason :- ΔE_g is more for GaAs.
(1) A (2) B (3) C (4) D

27. ***Assertion :-*** Photodiode always works under reverse bias condition. **[AIIMS-2017]**
Reason :- It is easier to detect current changes in reverse bias.
(1) A (2) B (3) C (4) D

28. ***Assertion :-*** GaAs can be used in making infrared LEDs.
Reason :- Its band gap lies between 1.8 eV to 3eV. **[AIIMS-2018]**
(1) A (2) B (3) C (4) D

EXERCISE-II (Assertion & Reason) ANSWER KEY

Que.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Ans.	**2**	**4**	**1**	**1**	**3**	**1**	**1**	**1**	**1**	**2**	**4**	**2**	**1**	**1**	**1**
Que.	16	17	18	19	20	21	22	23	24	25	26	27	28		
Ans.	**3**	**2**	**1**	**2**	**1**	**3**	**2**	**4**	**3**	**1**	**2**	**1**	**3**		